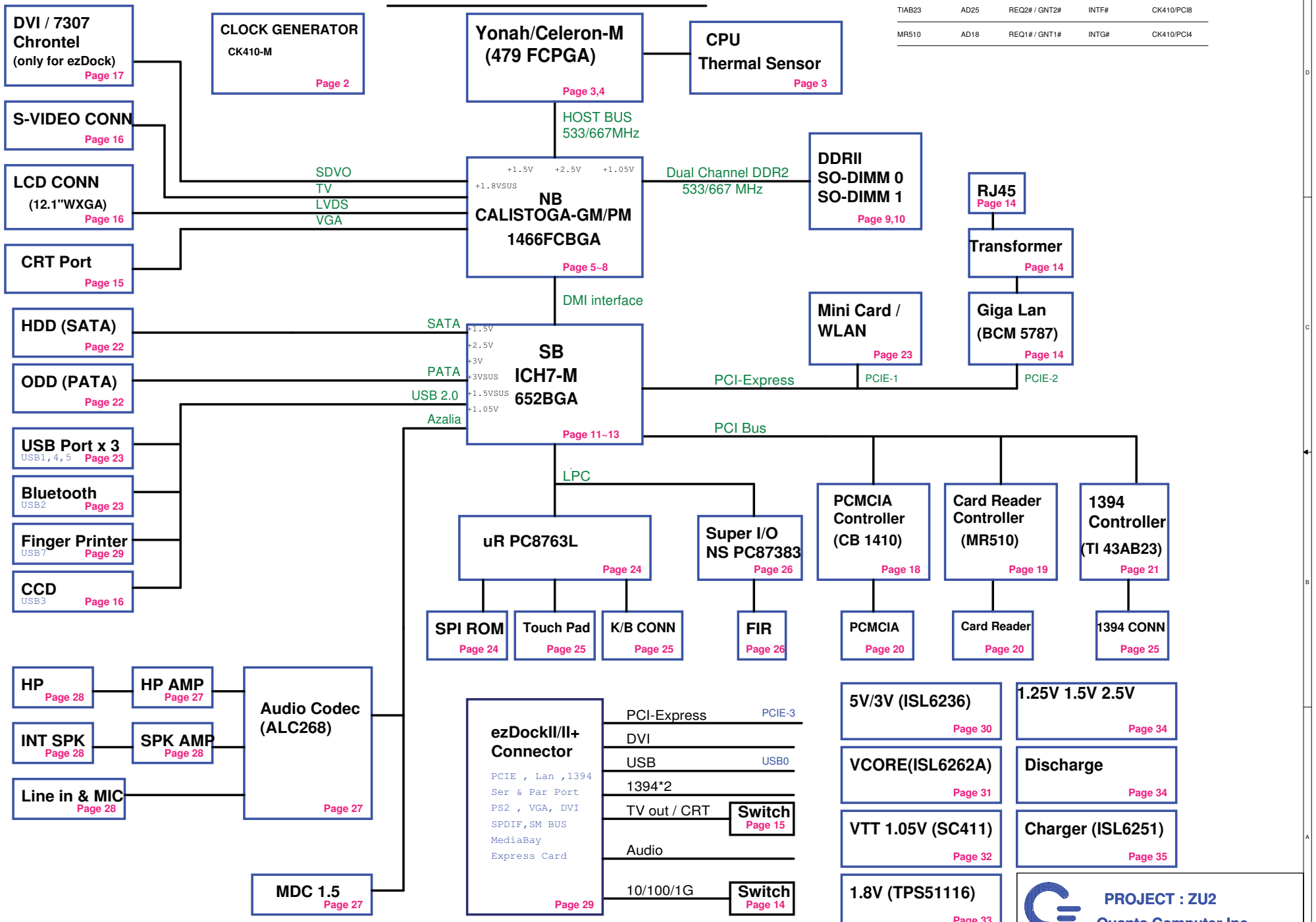
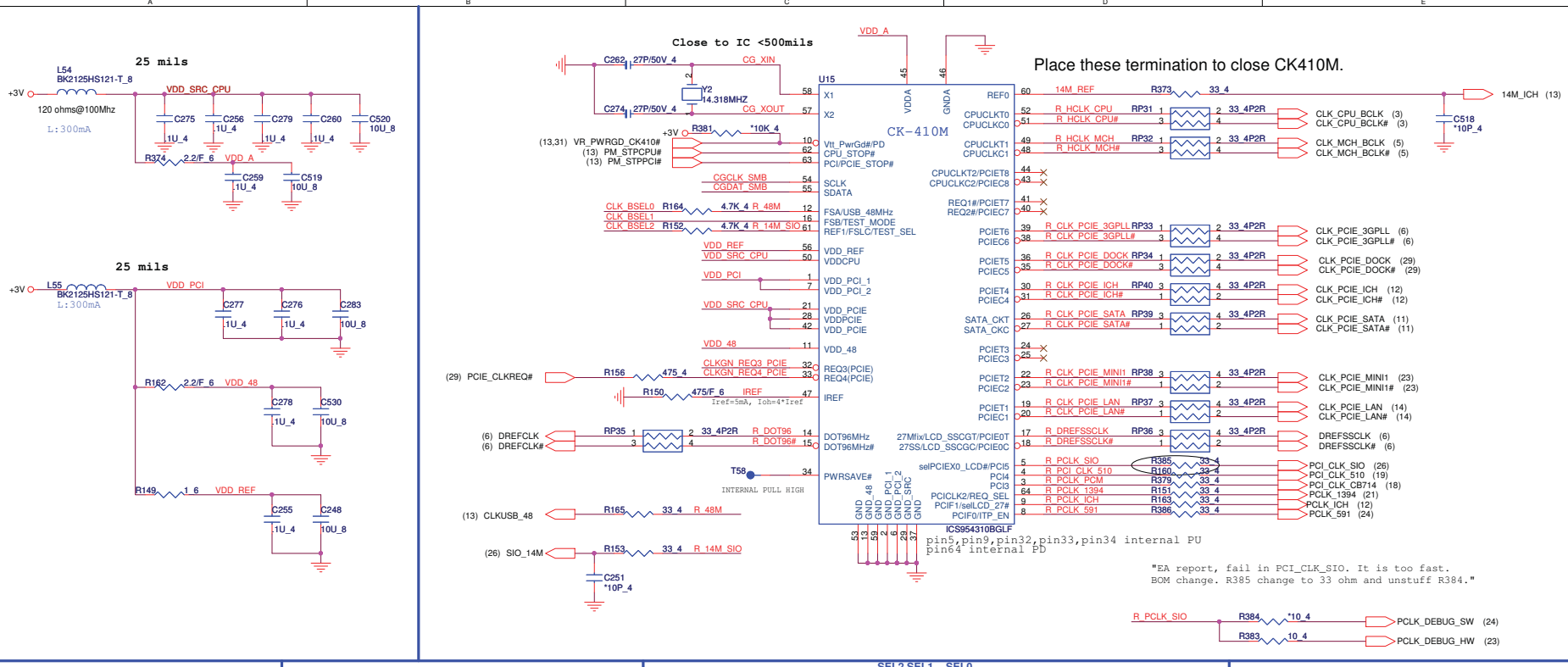
ZU2 SYSTEM BLOCK DIAGRAM

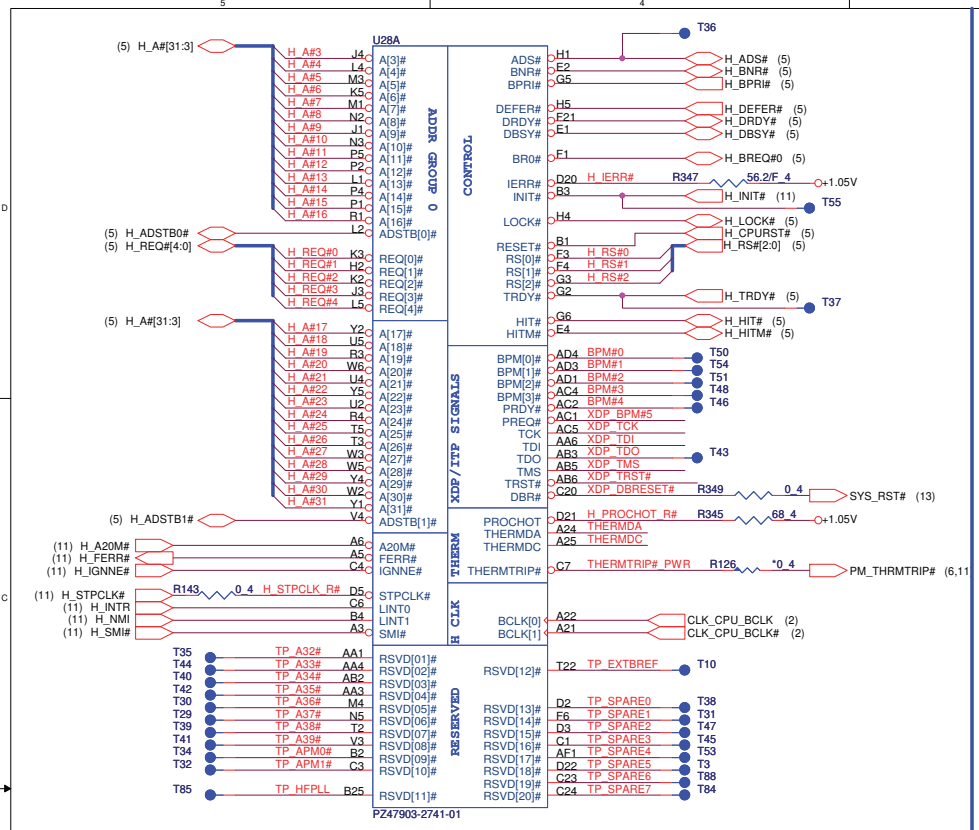
PCI DEVICE	IDSEL#	REQ# / GNT#	Interrupts	CLOCK
CB1410	AD17	REQ0# / GNT0#	INTE#	CK410/PCI3
TIAB23	AD25	REQ2# / GNT2#	INTF#	CK410/PCI8
MR510	AD18	REQ1# / GNT1#	INTG#	CK410/PCI4

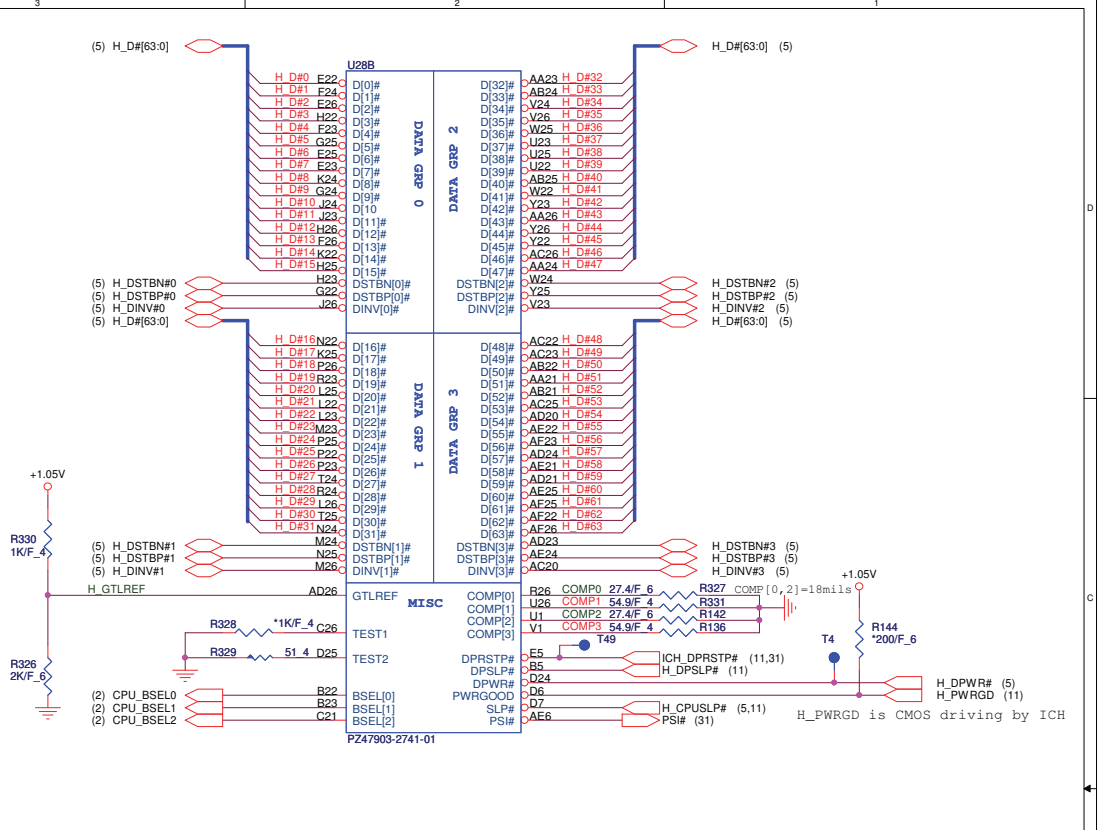


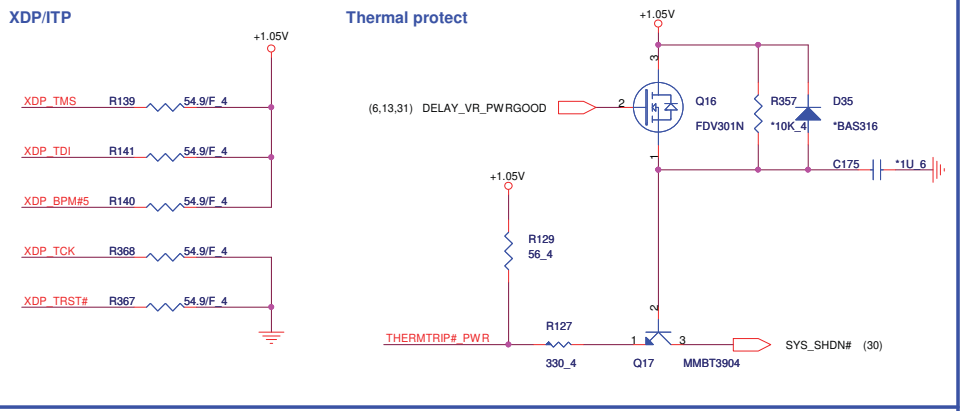
PROJECT : ZU2
Quanta Computer Inc.

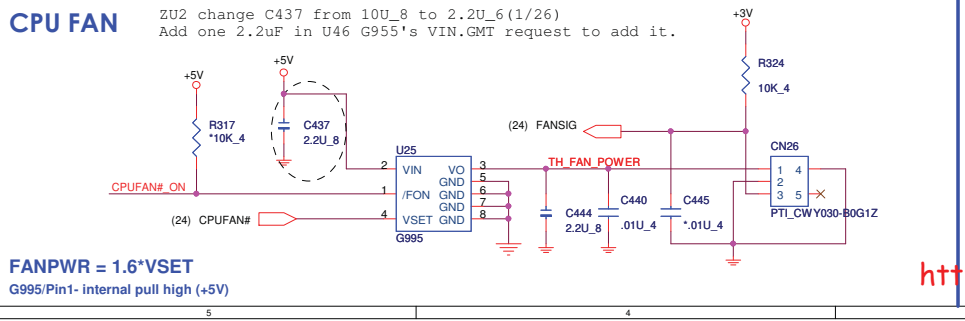
Size	Document Number	Rev
	Block Diagram	1A
Date: Wednesday, March 21, 2007	Sheet 1 of 39	

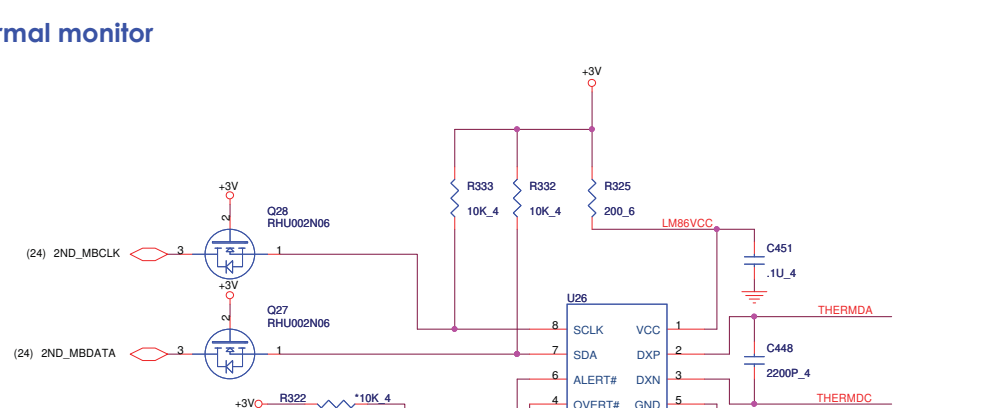








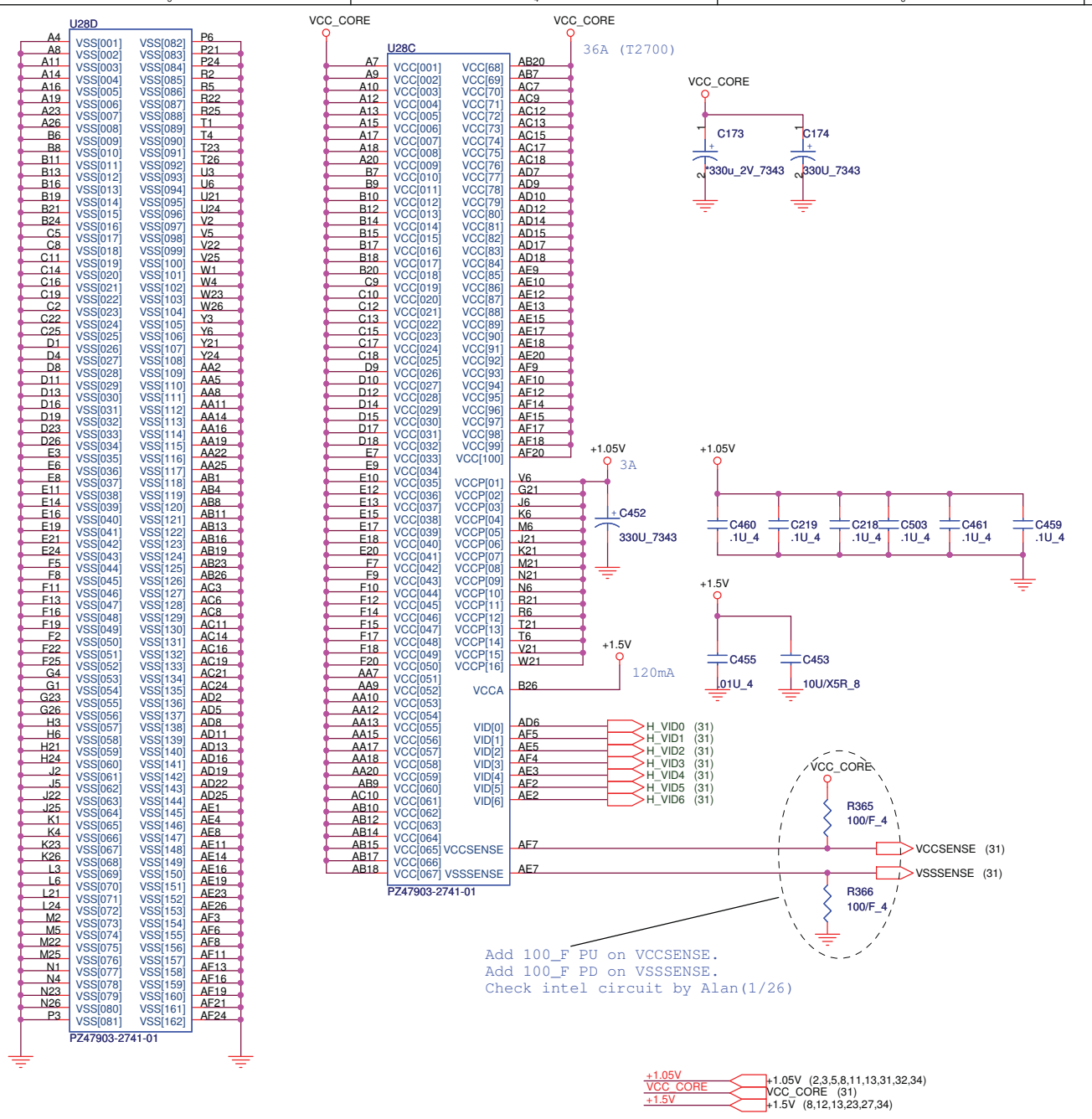




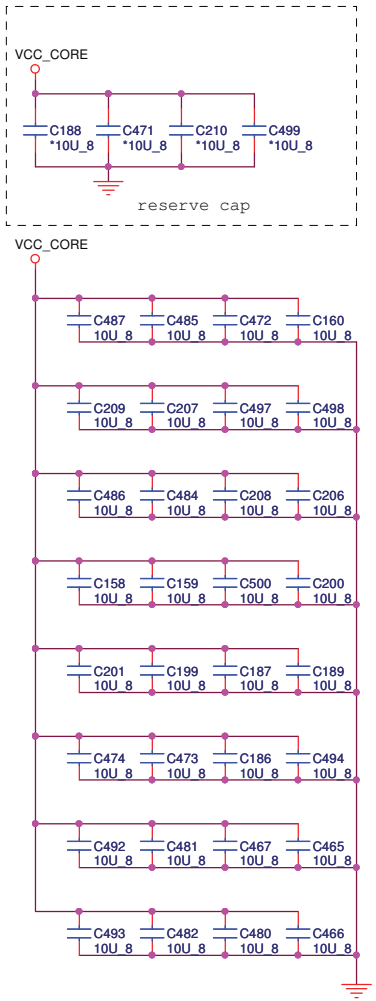
PROJECT : ZU2

Quanta Computer Inc.

Size	Document Number	Rev
	YOHNA (HOST)	1A
Date: Thursday, March 22, 2007	Sheet 3 of 39	



VCC_CORE CAP.



PROJECT : ZU2

Quanta Computer Inc.

Size	Document Number	Rev
	Yonah/Merom CPU(POWER/GND)-2	1A
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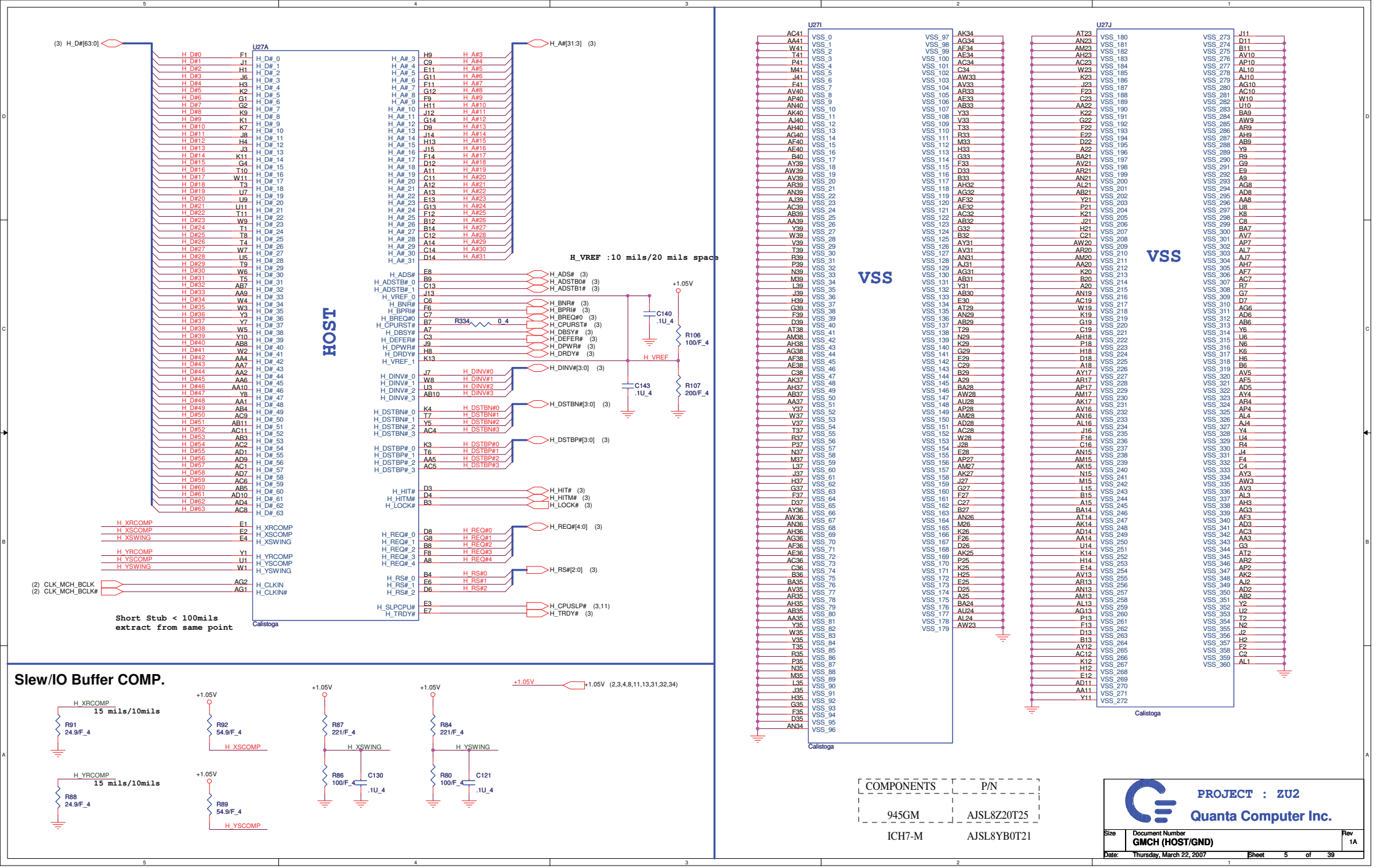

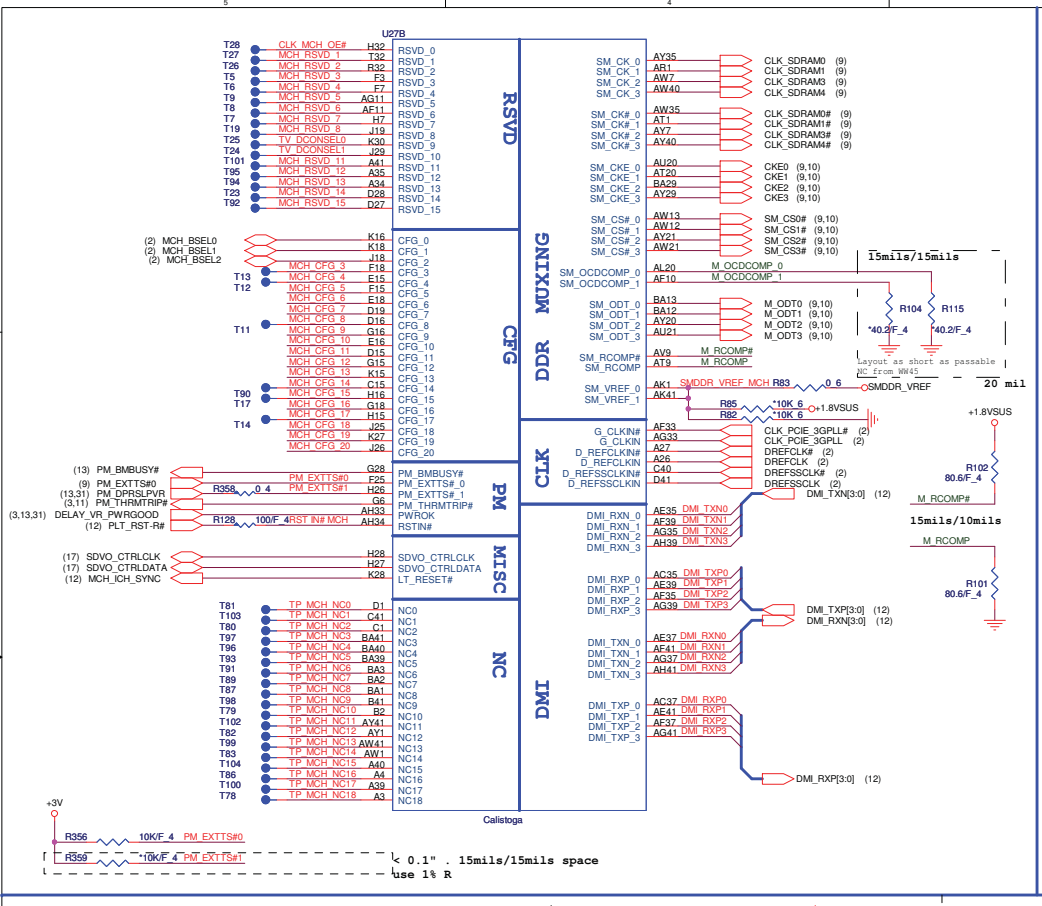

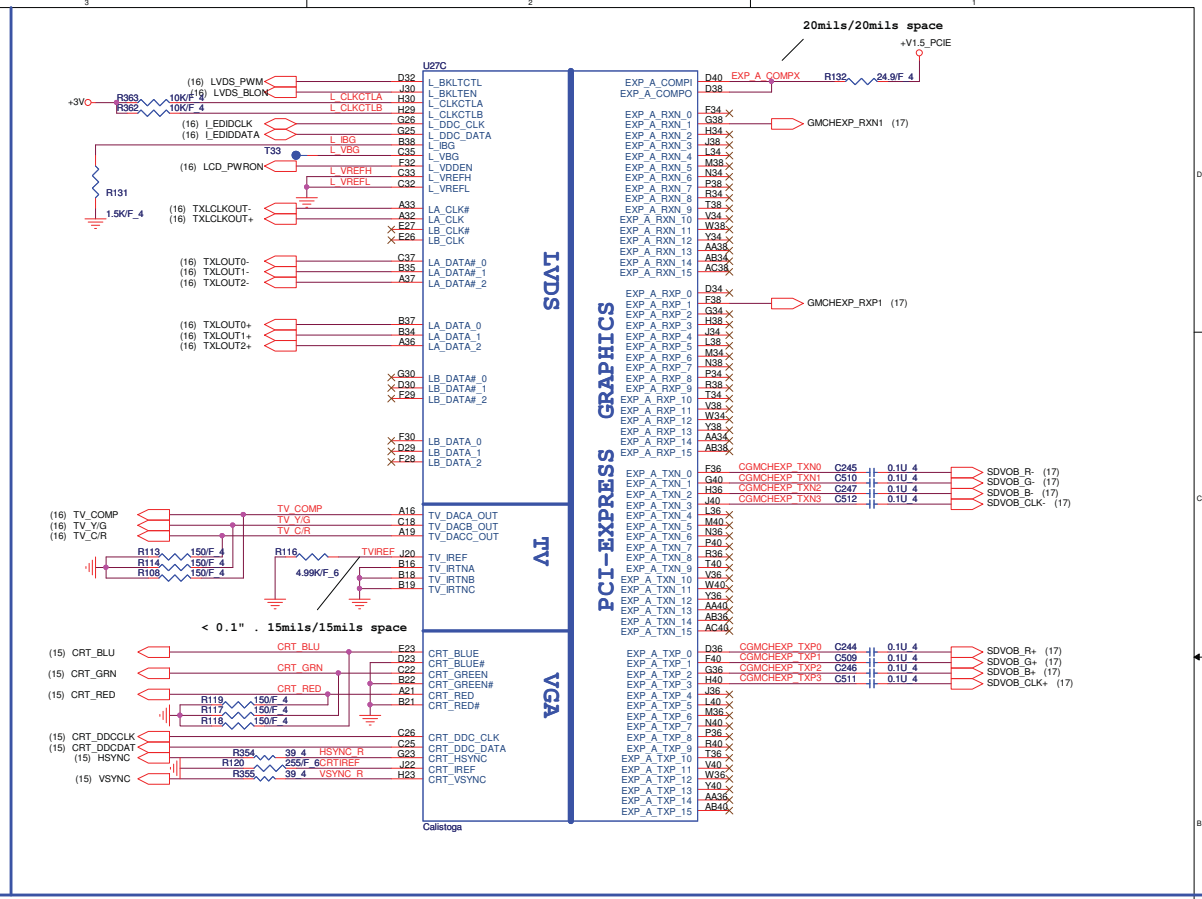

GMCH Strap pin

CFG[3..17] has internal PU

MCH_CFG_5 R341 *2.2K_4
MCH_CFG_5 DMI speed mode
Low = DMI X2
High=DMIX4

MCH_CFG_6 R348 *2.2K_4
MCH_CFG_6 DDR
Low =Moby Dick
High= Calistoga (Default)

MCH_CFG_7 R112 *2.2K_4
MCH_CFG_7 CPU Strap
Low=RSVD
High=Mobile CPU

MCH_CFG_9 R111 *2.2K_4
MCH_CFG_9 PCI Exp Graphics Lane
Low =Reserved
High=Normal

MCH_CFG_10 R346 *2.2K_4
MCH_CFG_10 Host PLL VCC Select
Low=Reserved
High=Mobility

MCH_CFG_11 R343 *2.2K_4
MCH_CFG_11 PSB 4x CLK ENABLE
Low=Reserved
High=Calistoga

MCH_CFG_12 R336 *2.2K_4
MCH_CFG_13 R109 *2.2K_4
MCH_CFG_12,13 XOR/ALLZ
0,0=Partial clock gating disable
0,1=All-Z mode enable
1,0=XOR mode enable
1,1=Normal

MCH_CFG_16 R344 *2.2K_4
MCH_CFG_16 FSB Dynmic ODT
Low=Dynamic ODT Disabled
High=Dynamic ODT Enabled.

CFG[18..20] has internal PD

MCH_CFG_18 R360 *1K/F_4 +3V
MCH_CFG_18 VCC Select
LOW=1.05V
High=1.5V

MCH_CFG_19 R361 *1K/F_4 +3V
MCH_CFG_19 DMI LANE Reversal
Low=Normal
High=LANES Reversed

MCH_CFG_20 R364 *1K/F_4 +3V
MCH_CFG_20 PCIE Backward interpoerability mode
Low= only SDVO or PCIE x1 is operational (defaults)
High=SDVO and PCIE x1 are operation simultaneously via the PEG port

+V1.5_PCIE (8)
+3V (2,3,8,9,11,12,13,14,15,16,17,18,19,20,21,22,23,24,25,26,27,29,30,31,32,34)
SMDDR_VREF (9,33,34)
+1.8VSUS (8,9,33,34)

PROJECT : ZU2
Quanta Computer Inc.

Size	Document Number	Rev
	GMCH (DMI&PCIE&VGA)	1A
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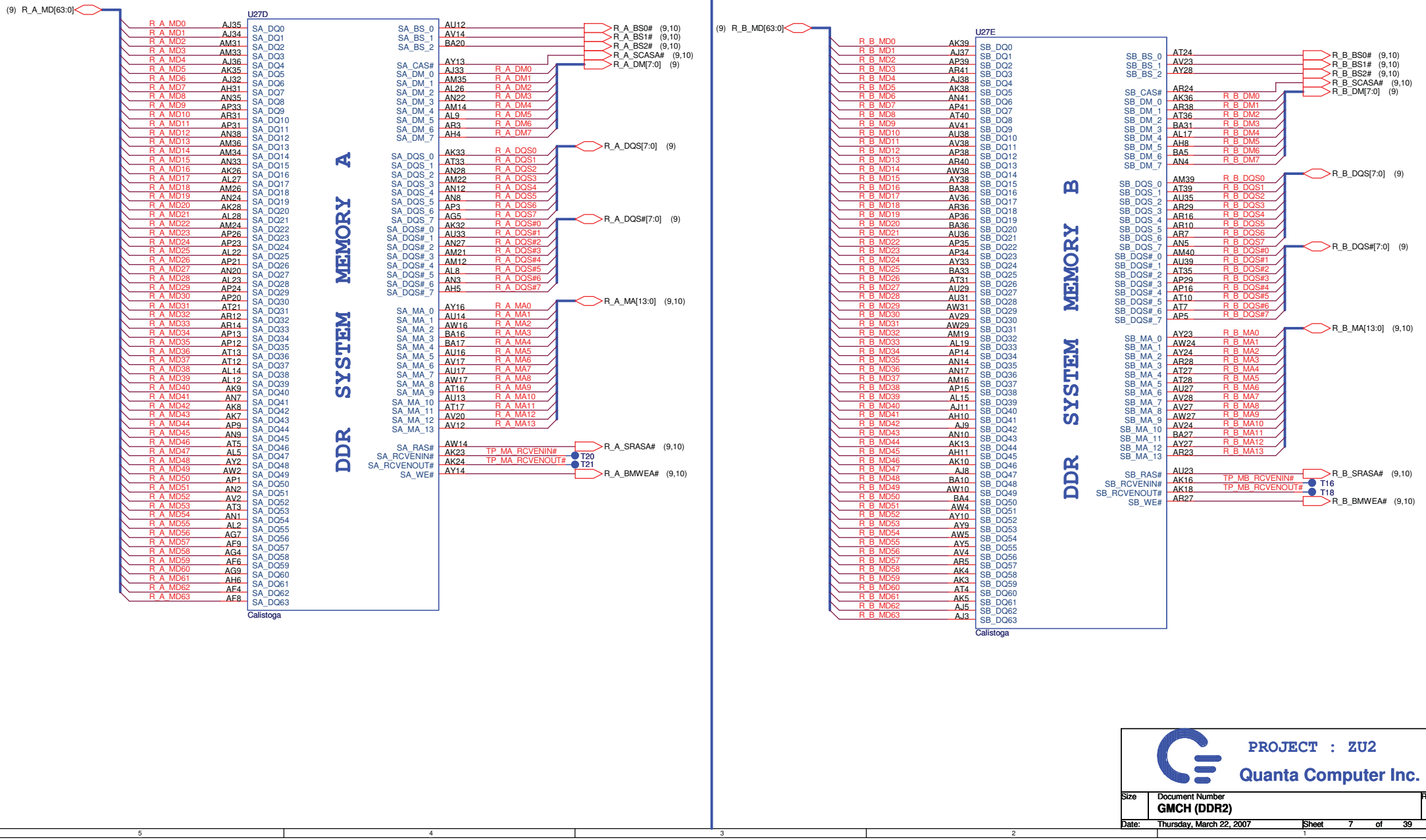
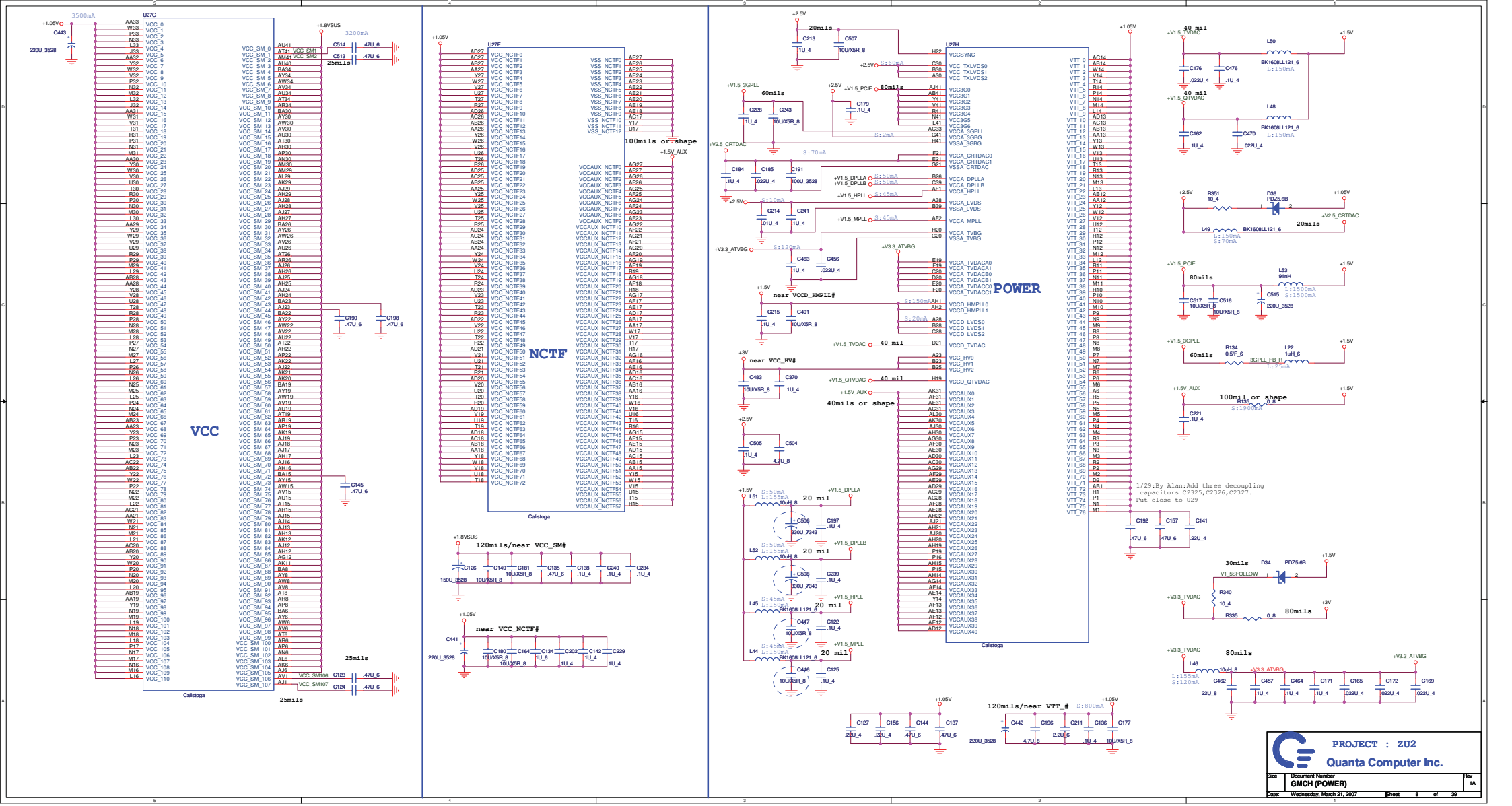
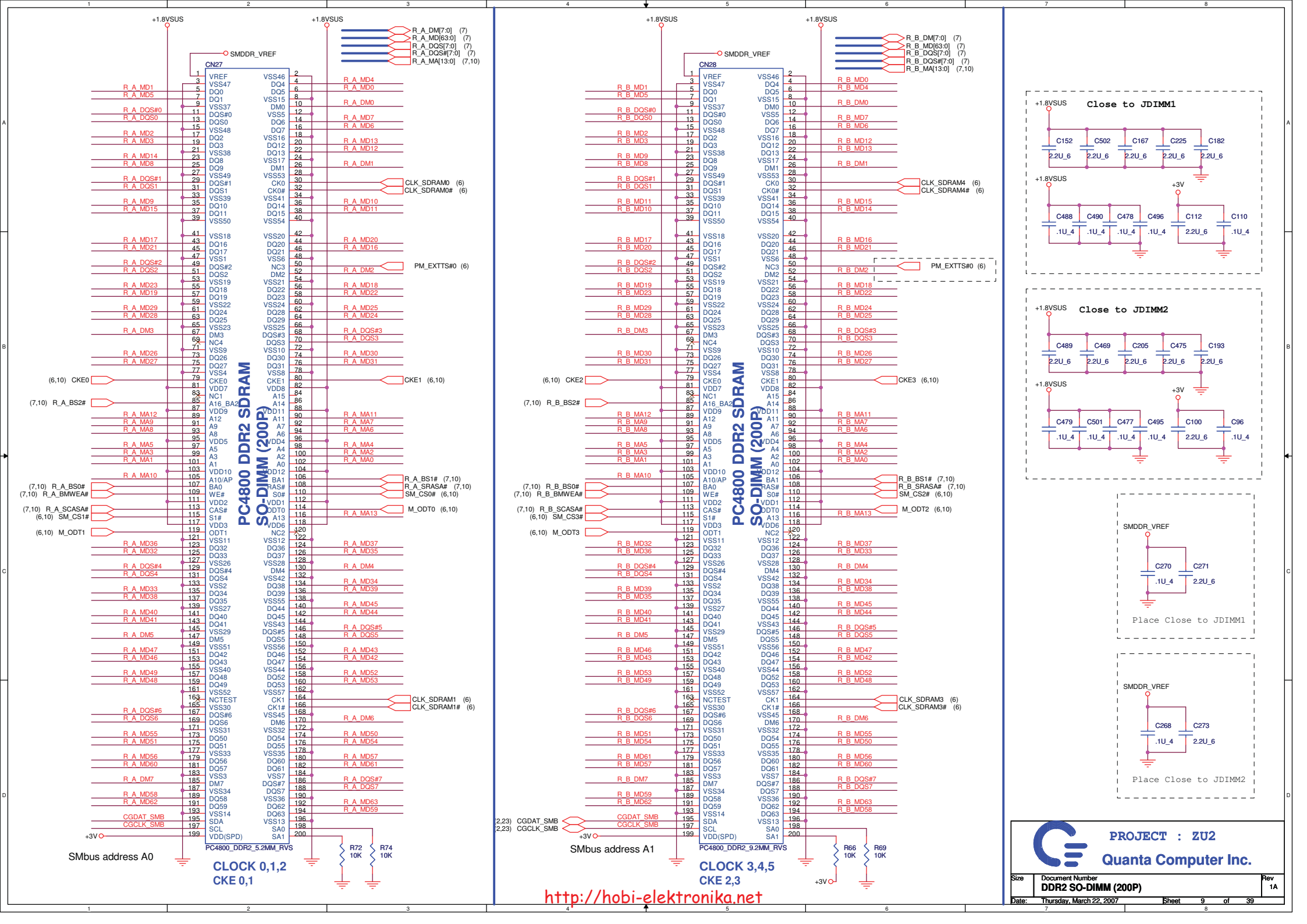


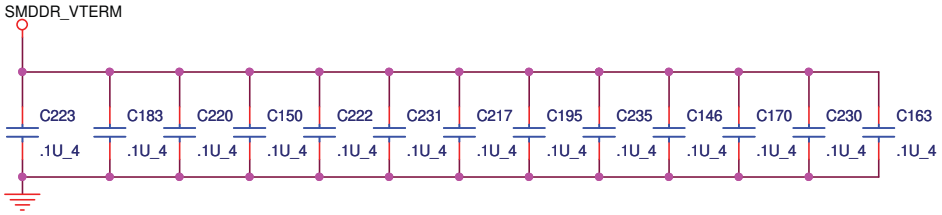
PROJECT : ZU2

Quanta Computer Inc.

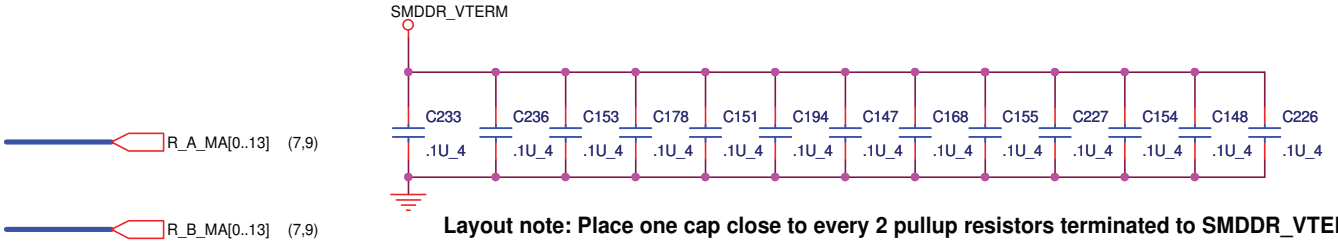
Size	Document Number	Rev
	GMCH (DDR2)	1A
Date: Thursday, March 22, 2007	Sheet 7 of 39	


VCC
NCTF
POWER
Calistoga
Calistoga
Calistoga
PROJECT : ZU2
Quanta Computer Inc.
GMCH (POWER)
Wednesday, March 21, 2007
http://hobi-elektronika.net

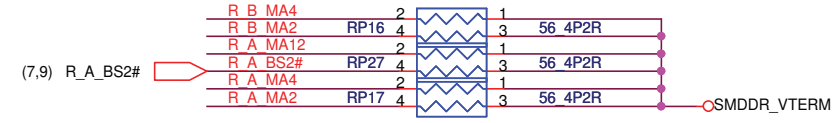


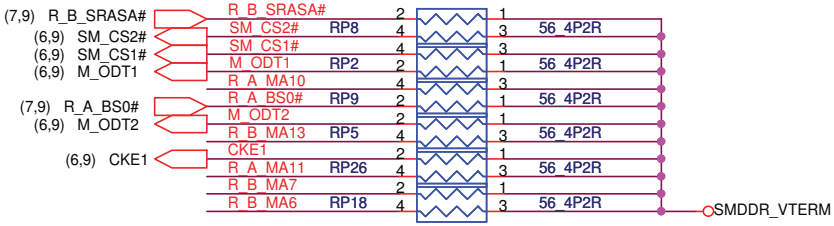


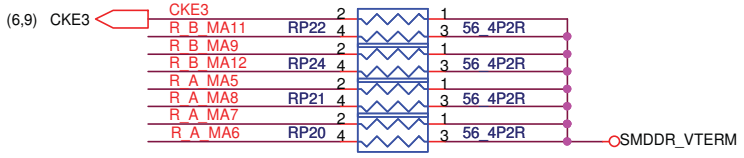
Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM

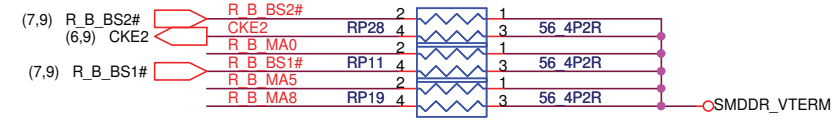


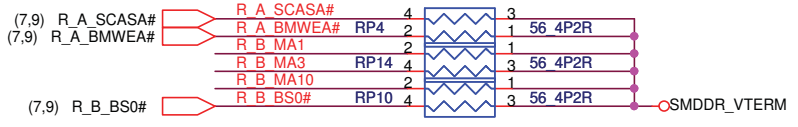
Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM

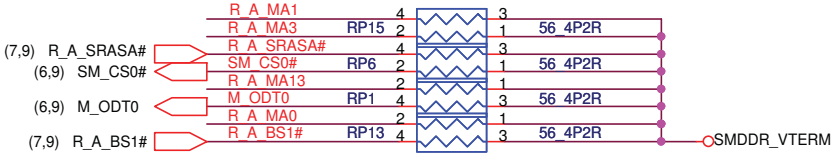












PROJECT : ZU2

Quanta Computer Inc.

Size	Document Number	Rev
	DDR2 RES. ARRAY	1A
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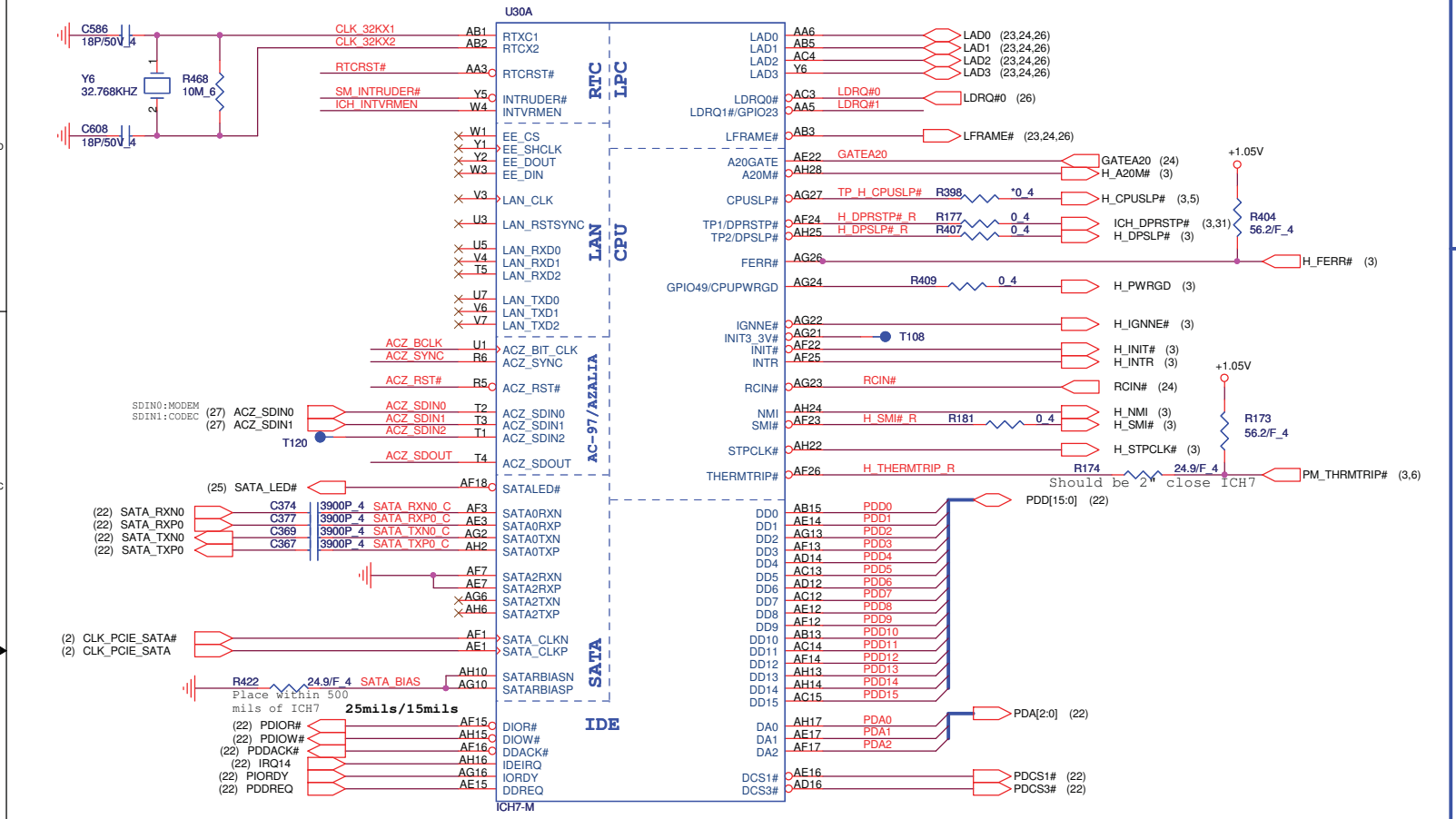
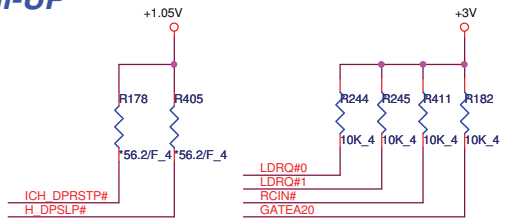
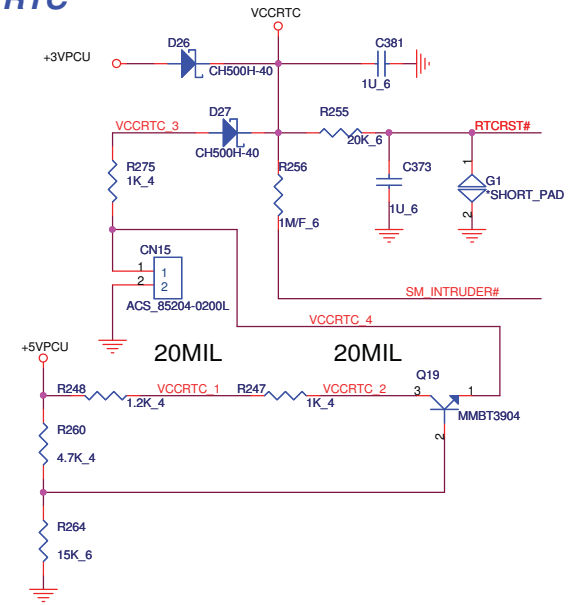


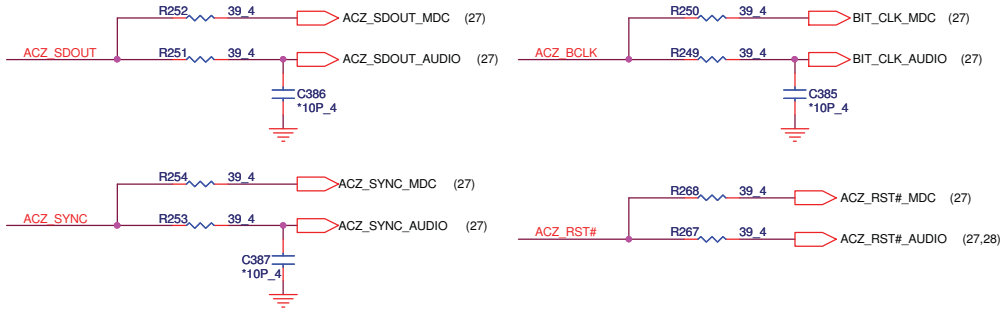
Pull-UP



RTC



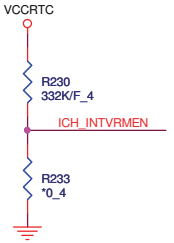
HDA interface



COMPONENTS	P/N
945GM	AJSL8Z20T25
ICH7-M	AJSL8YB0T21

ICH7 internal VR enable strap

	INTVRMEN
Enable (default)	1
Disable	0



PROJECT : ZU2

Quanta Computer Inc.

Size	Document Number	Rev
	ICH7-M (CPU, SATA, IDE,LPC)	1A
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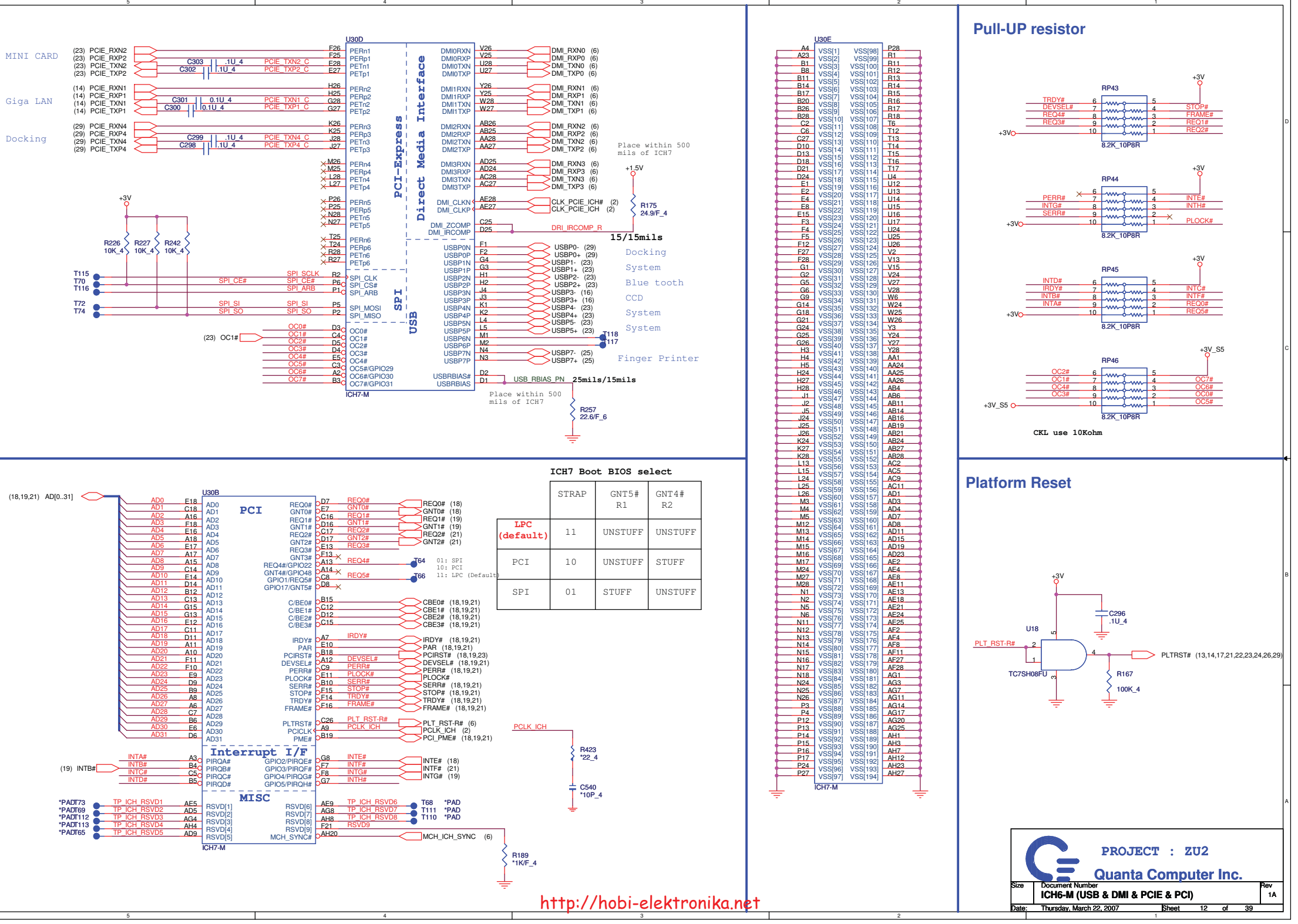
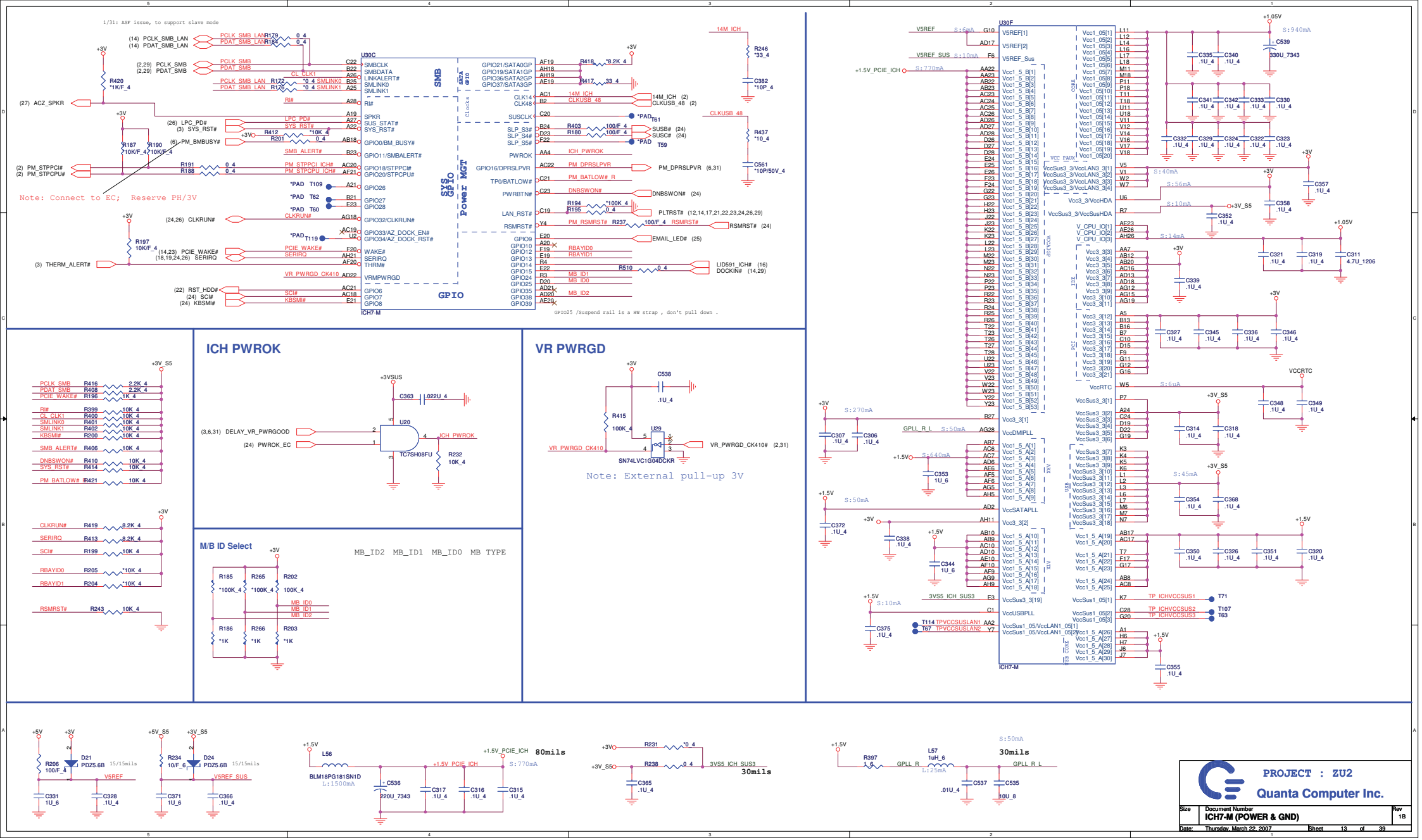
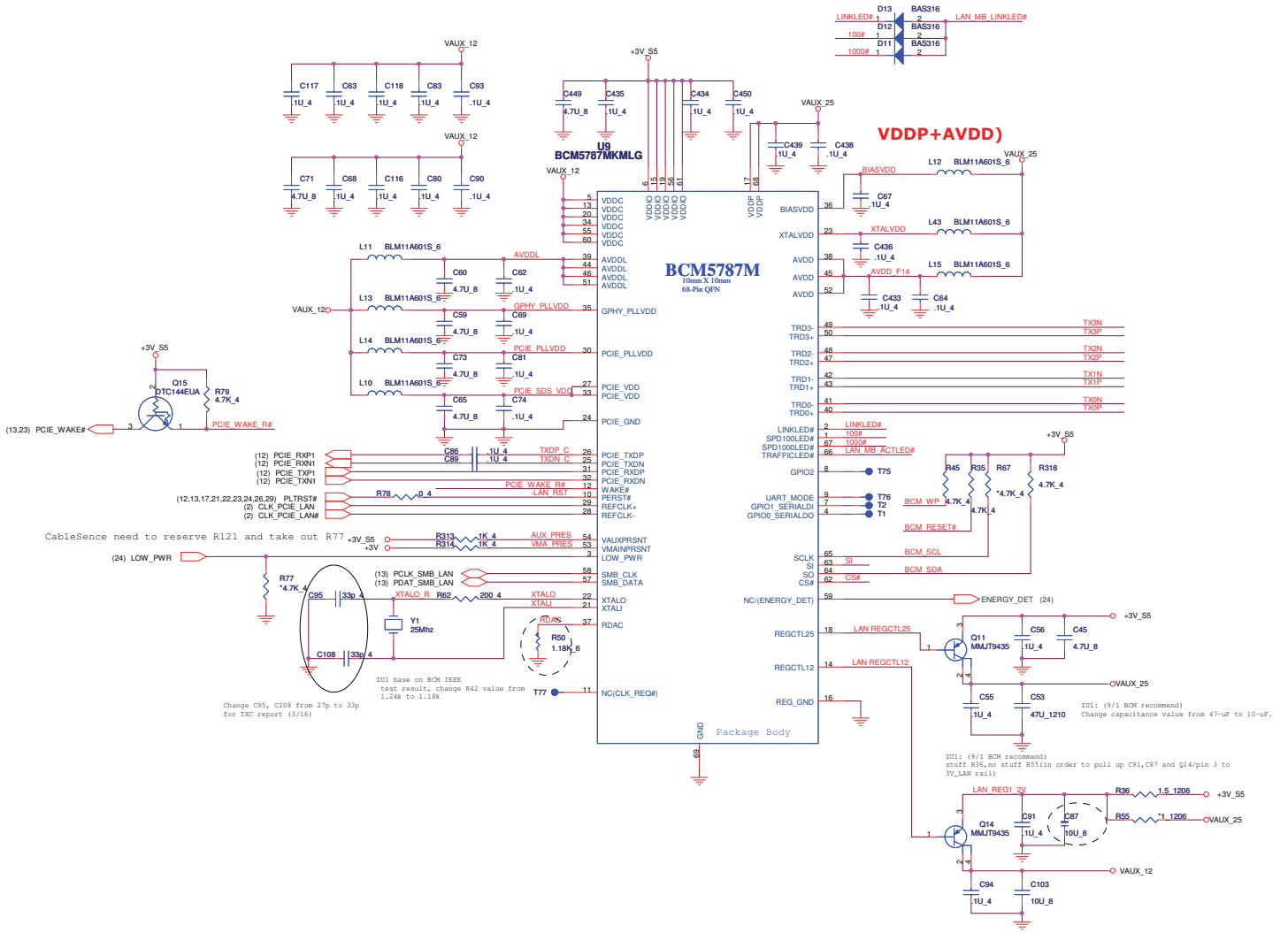


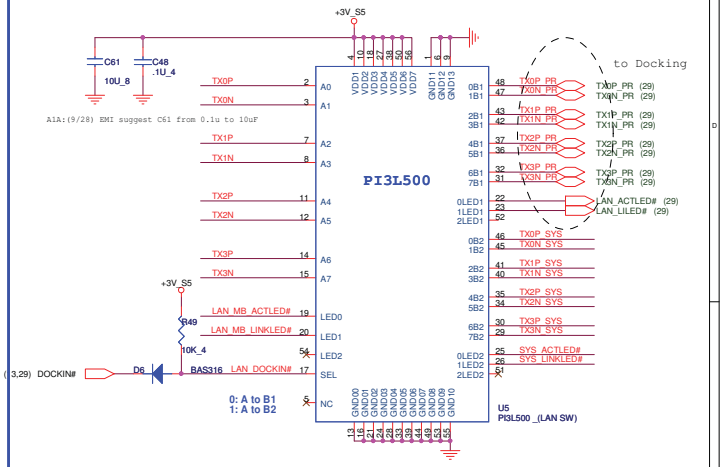
	STRAP	GNT5# R1	GNT4# R2
LPC (default)	11	UNSTUFF	UNSTUFF
PCI	10	UNSTUFF	STUFF
SPI	01	STUFF	UNSTUFF



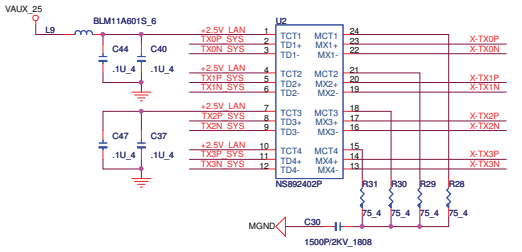
Giga LAN BCN5787M



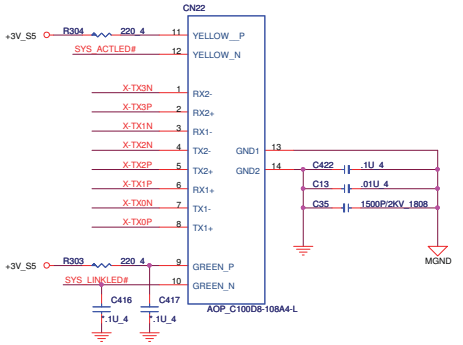
LAN Switch



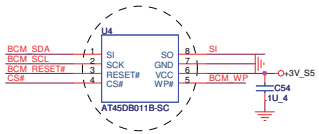
LAN Transformer



RJ45

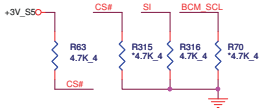


Flash ROM/EEPROM



EEPROM Strapping

	SO	SI	CS#	SCLK
24c64	1	1	0	1
AT45DB011B	1	0	1	1



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Quanta Computer Inc.

Size	Document Number	Rev
	GigaLAN (BCM5787M) / RJ45	1B

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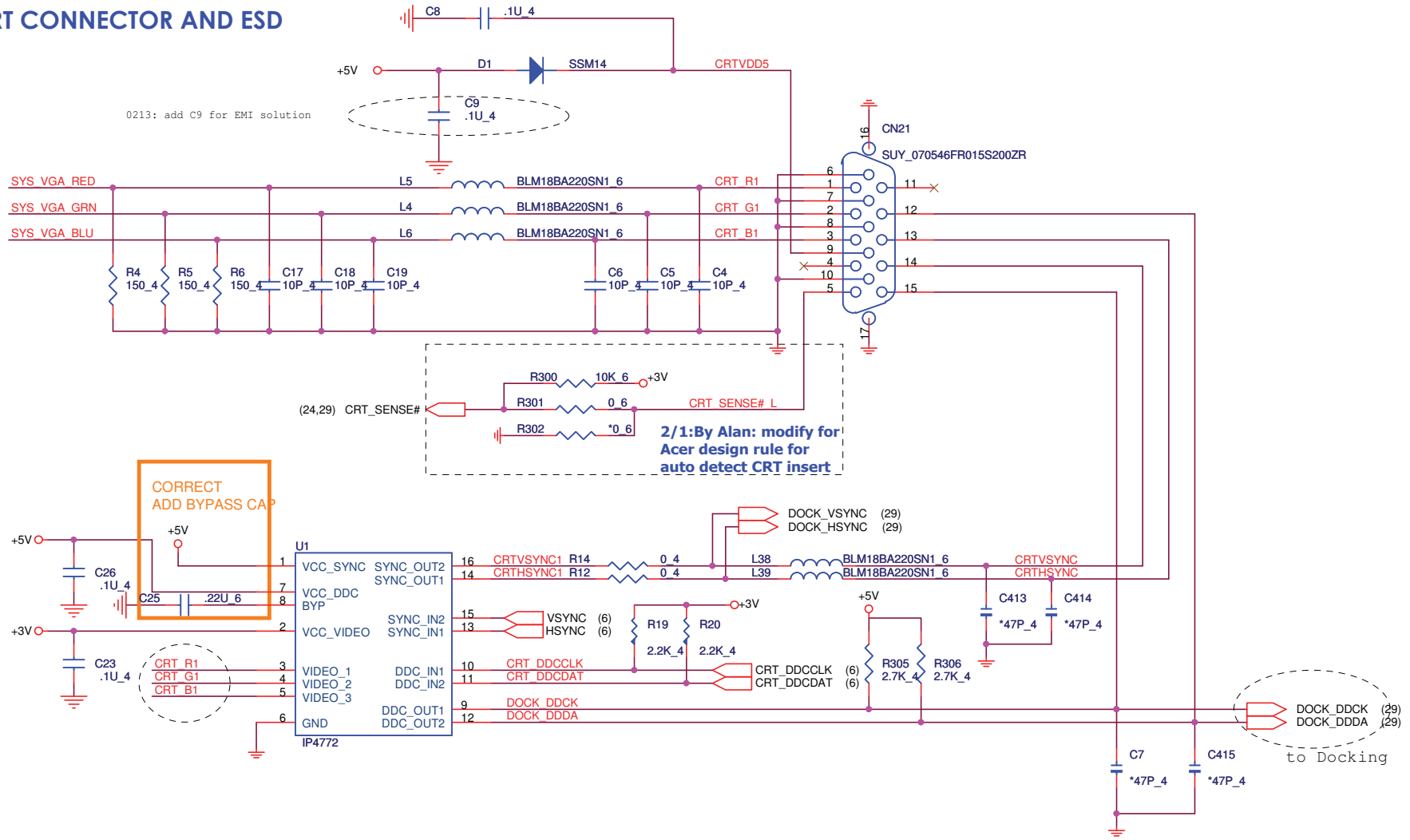
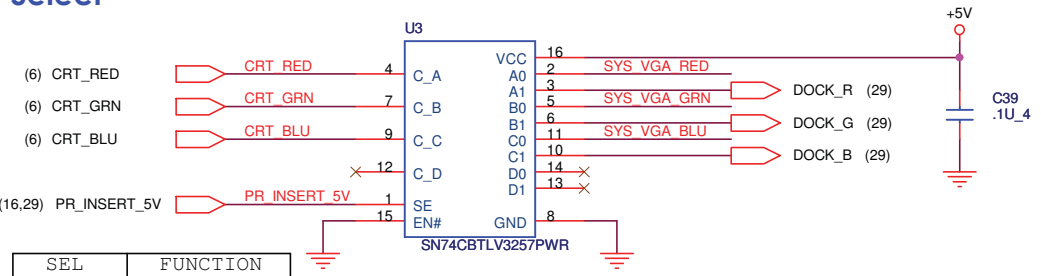
CRT CONNECTOR AND ESD



CRT Select



SEL	FUNCTION
LOW	IN_0
HIGH	IN_1

PROJECT : ZU2

Quanta Computer Inc.

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	CRT	1A
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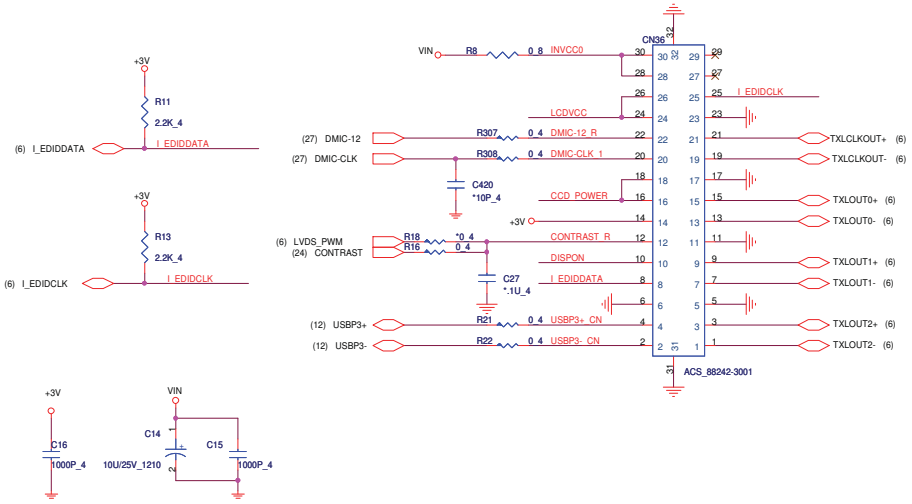
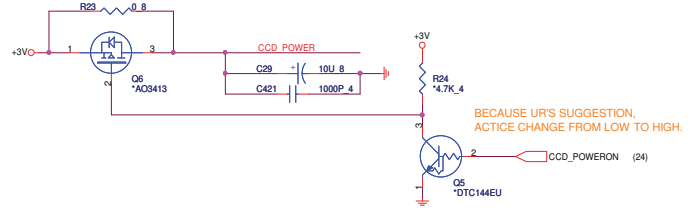
LVDS



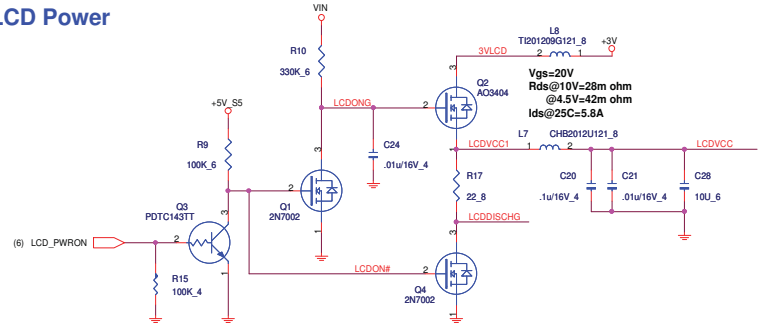
ZU1:(12/28) EMI request: reserve L-C footprint for debug use (R52,C650)

(3/19)Change MB LCD connector pin define(CN3) and LCD cable pin define to cover production line issue
(Inverter short with signal to burn system)->ZR1 issue
(1)pin 27,29->NC
(2)pin 8->INT_LVDS_EDIDDATA

CAMERA MODULE

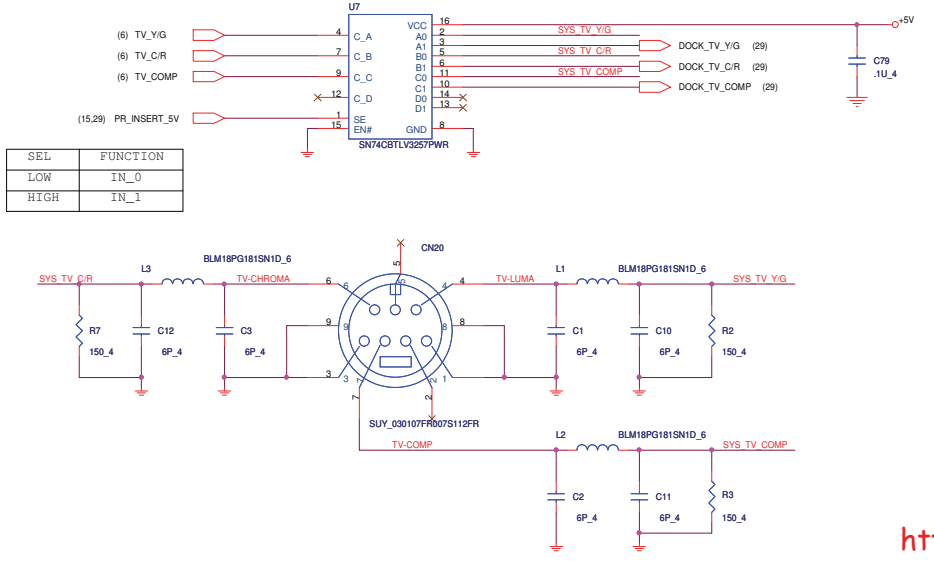


LCD Power

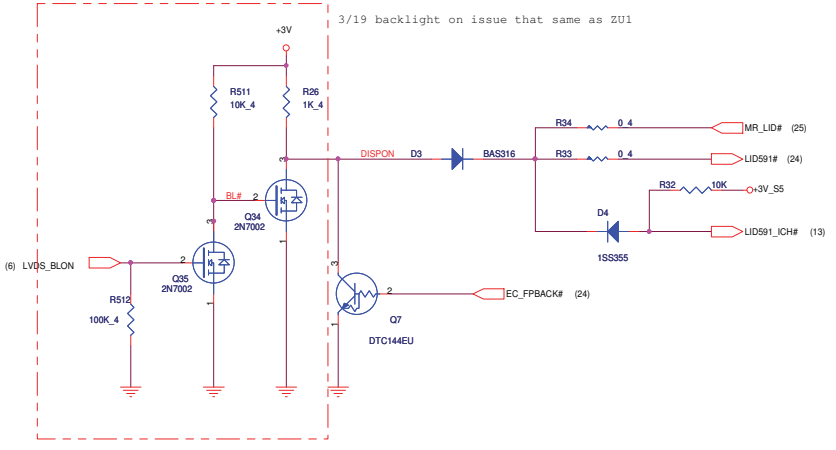


1/29:By Alan: AAT4280 fail on power ON rising time and falling time. EA.Additionally, some LCD panels will have garbage. follow ZR1 circuit.

TV Out (SVHS) MiniDIN 7-pin



MR Sensor



PROJECT : ZU2
Quanta Computer Inc.

Size	Document Number	Rev
	LVDS/MR senseor/SVIDEO	1B
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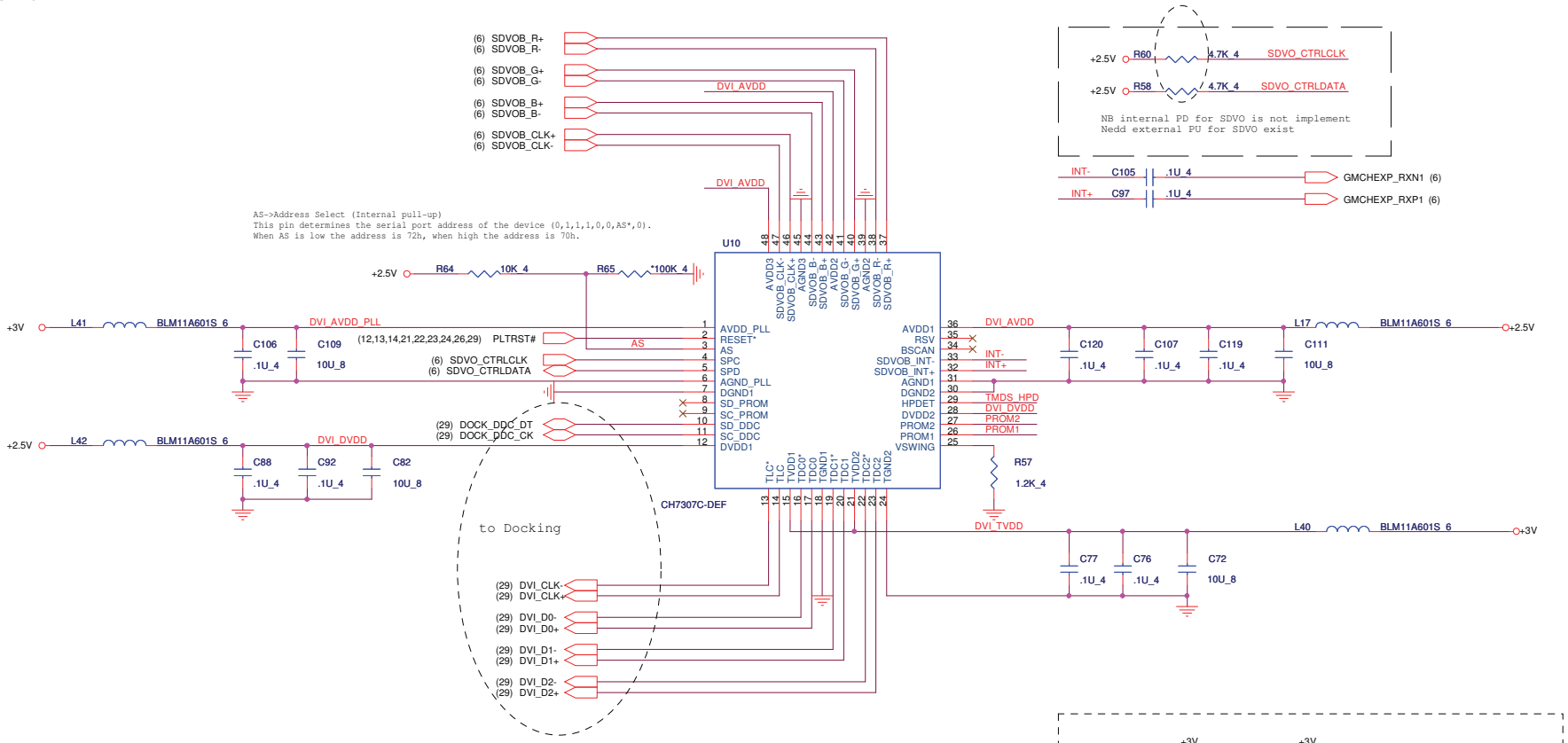
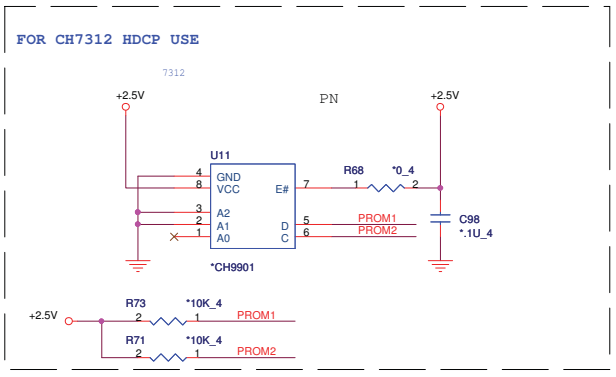
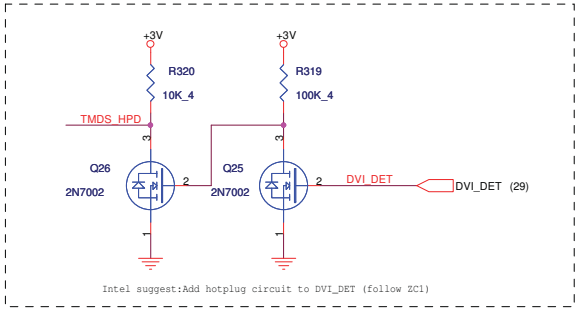
SDVO-DVI







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Quanta Computer Inc.

Size	Document Number	Rev
	DVI (CH7307)	1A
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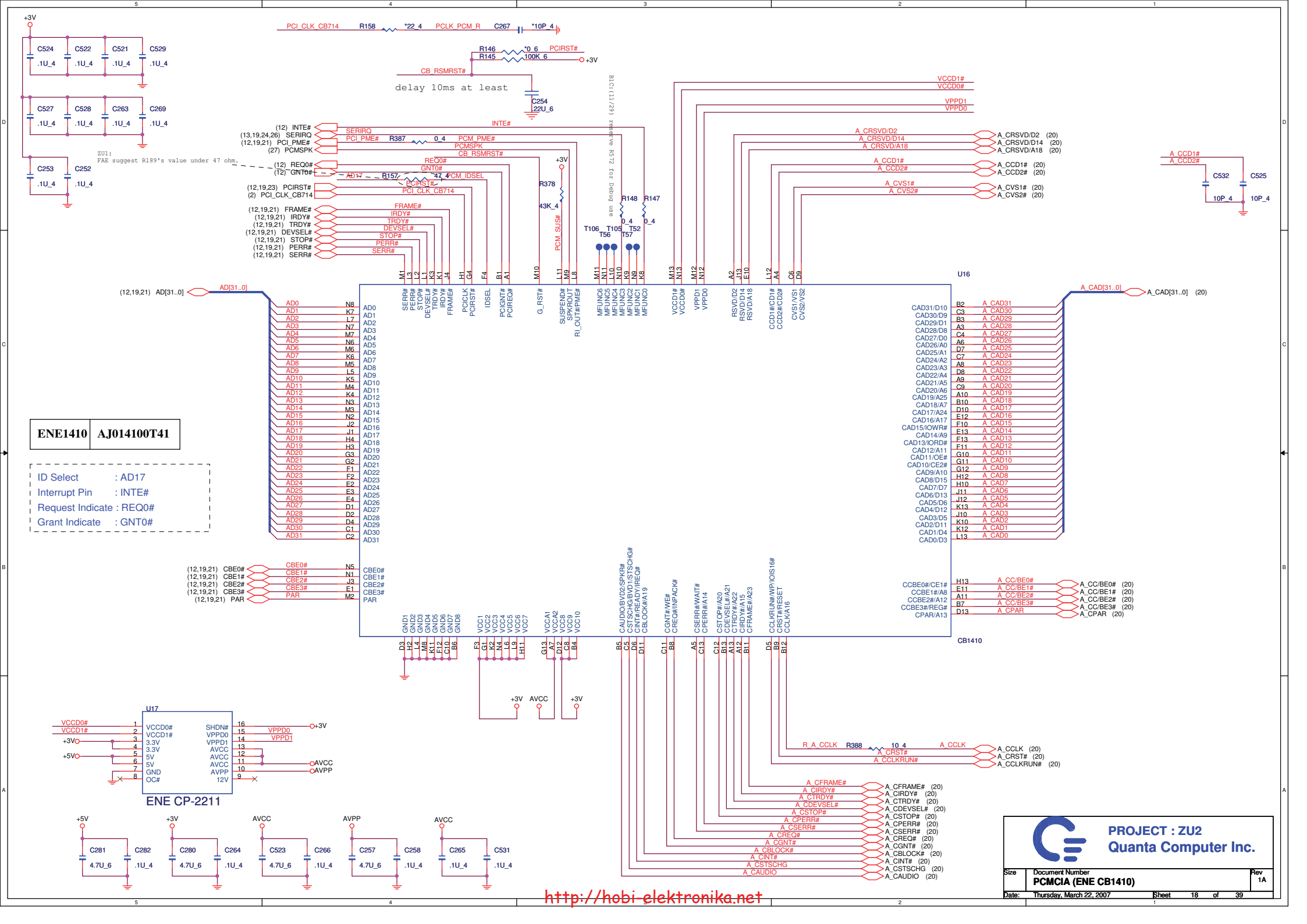

ENE1410 AJ014100T41
ID Select : AD17
Interrupt Pin : INTE#
Request Indicate : REQ0#
Grant Indicate : GNT0#
CB1410
ENE CP-2211
U16
U17
delay 10ms at least
ZU1:
FAE suggest R189's value under 47 ohm.
PROJECT : ZU2
Quanta Computer Inc.
PCMCIA (ENE CB1410)
Thursday, March 22, 2007
http://hobi-elektronika.net

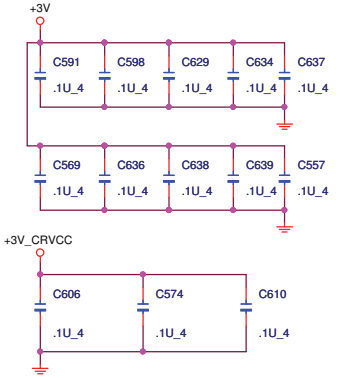
ID Select : AD18
Interrupt Pin : INTG#
Request Indicate : REQ1#
Grant Indicate : GNT1#

ZU1:no stuff R496,R522

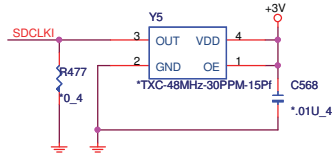
GRST# should connect to Power On reset if support S3

ZU1:FAE suggest R value under 47 ohm.

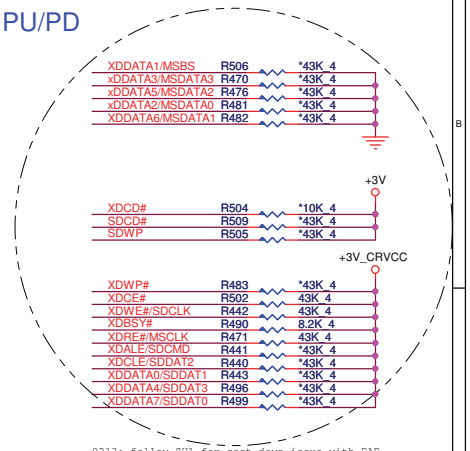
Decoupling CAP.



48MHz CLK



PU/PD

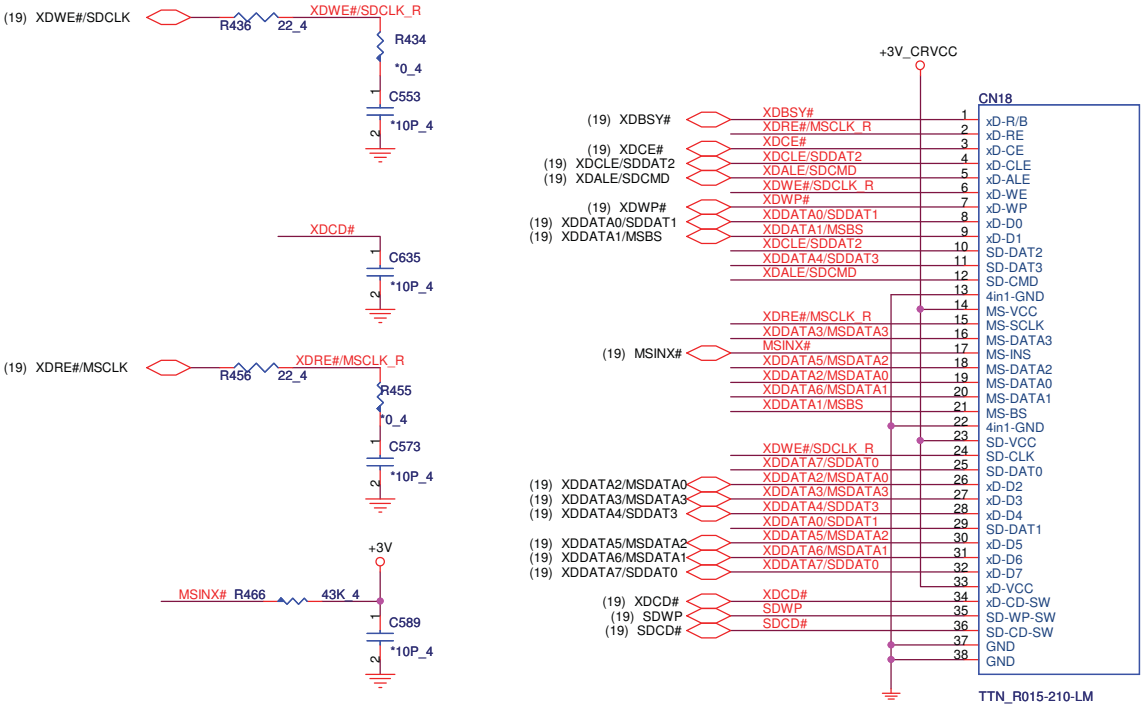


0213: follow ZU1 for cost down issue with FAE

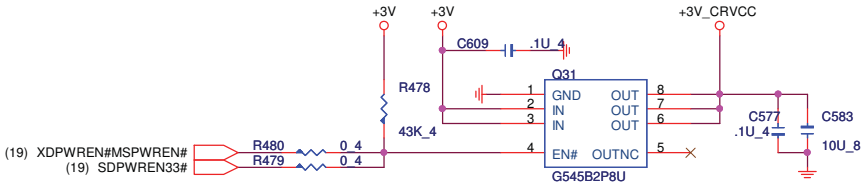
PROJECT : ZU2
Quanta Computer Inc.

Size	Document Number	Rev
	Card Reader (MR510)	1B
Date: Wednesday, March 28, 2007	Sheet 19 of 39	

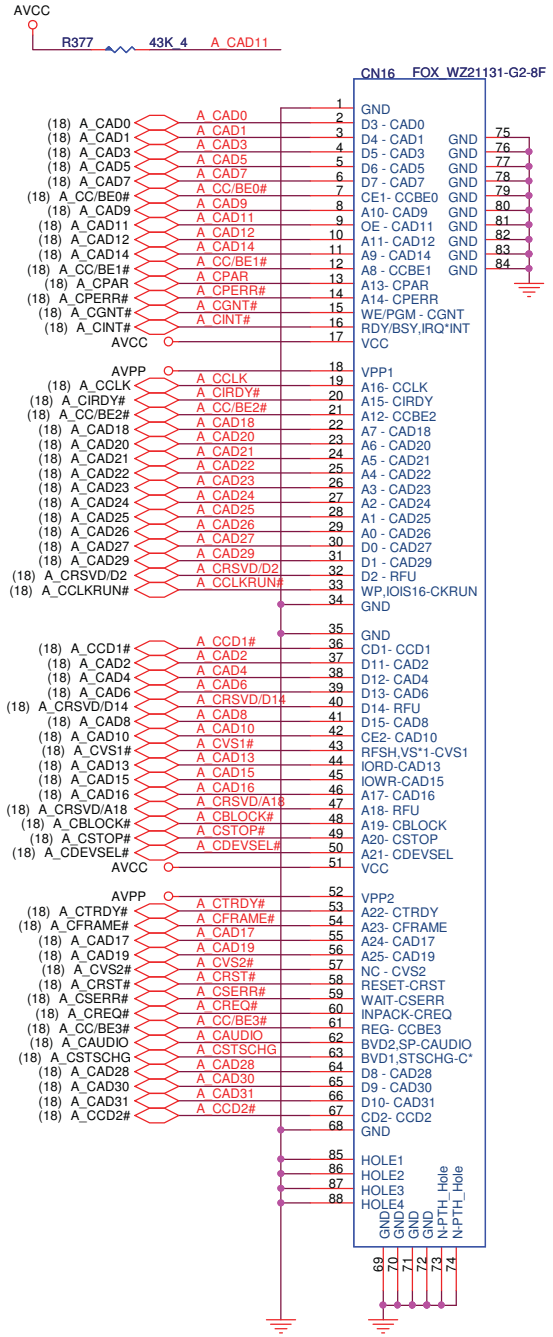
CardReader



CardReader Power switch



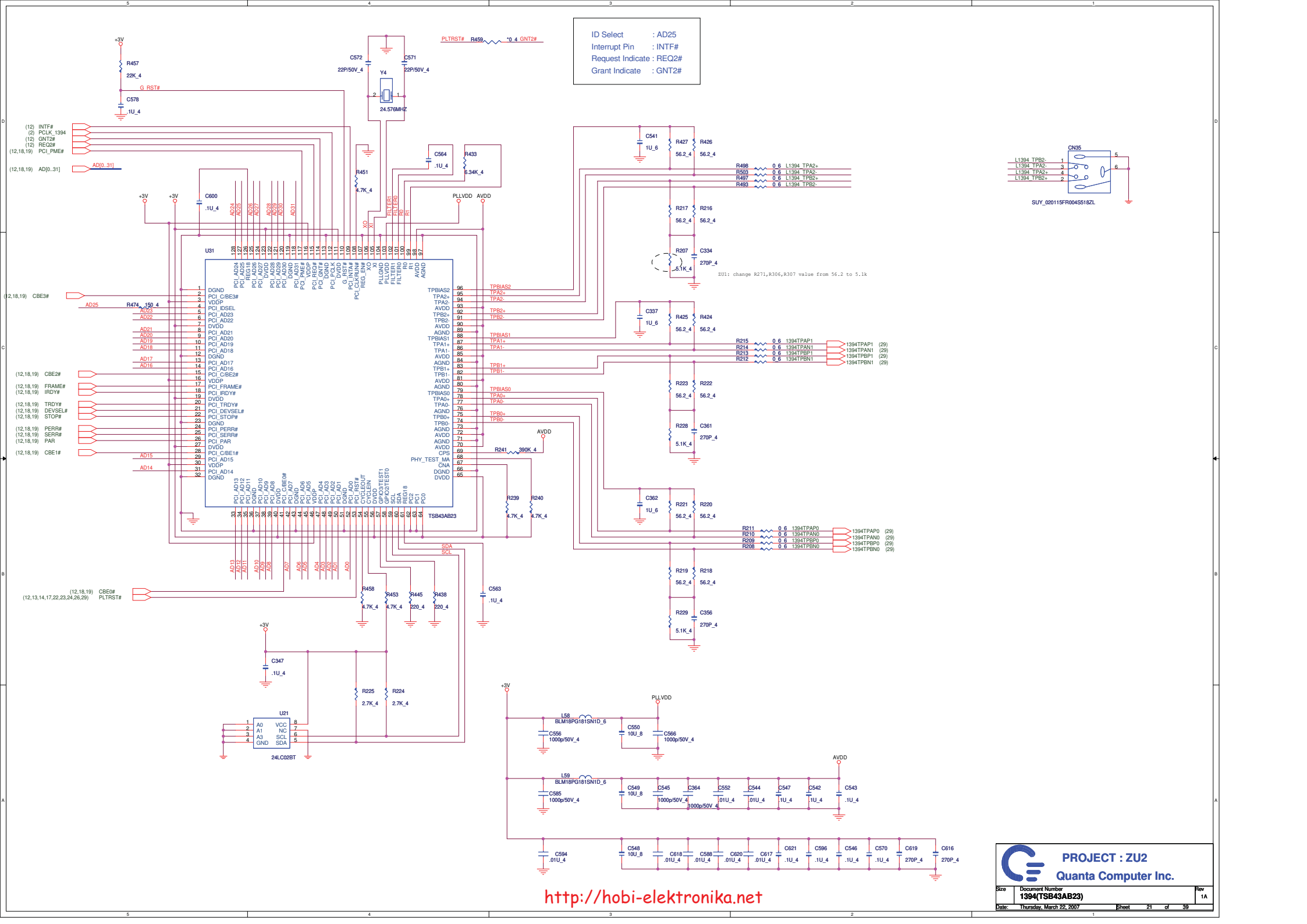
PCMCIA



PROJECT : ZU2

Quanta Computer Inc.

Size	Document Number	Rev
	CARD Reader & PCMCIA SLOT	1A
Date: Thursday, March 22, 2007	Sheet 20 of 39	


ID Select : AD25
Interrupt Pin : INTF#
Request Indicate : REQ2#
Grant Indicate : GNT2#
U31
TSB43AB23
U21
24LC02BT
CN35
SUY_020115FR004S518ZL
ZU1: change R271,R306,R307 value from 56.2 to 5.1k
PROJECT : ZU2
Quanta Computer Inc.
Size
Document Number
1394(TSB43AB23)
Rev
1A
Date: Thursday, March 22, 2007
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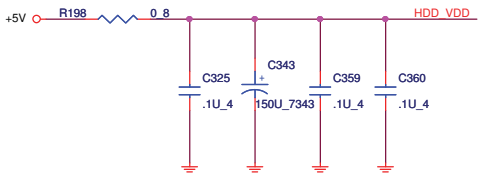
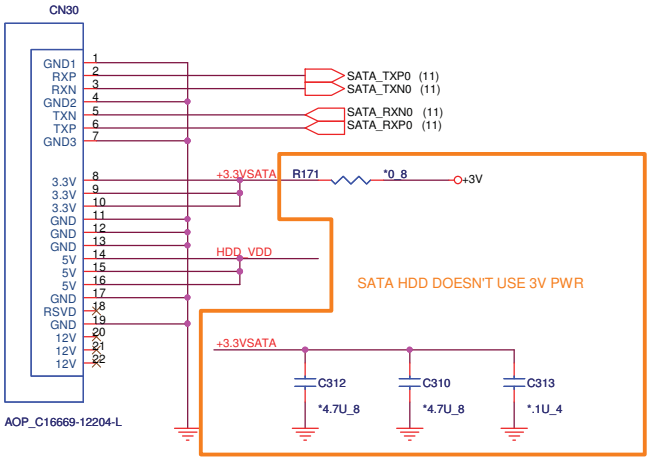
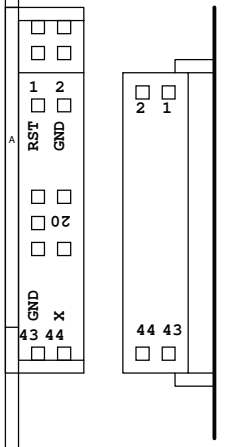
http://hobi-elektronika.net

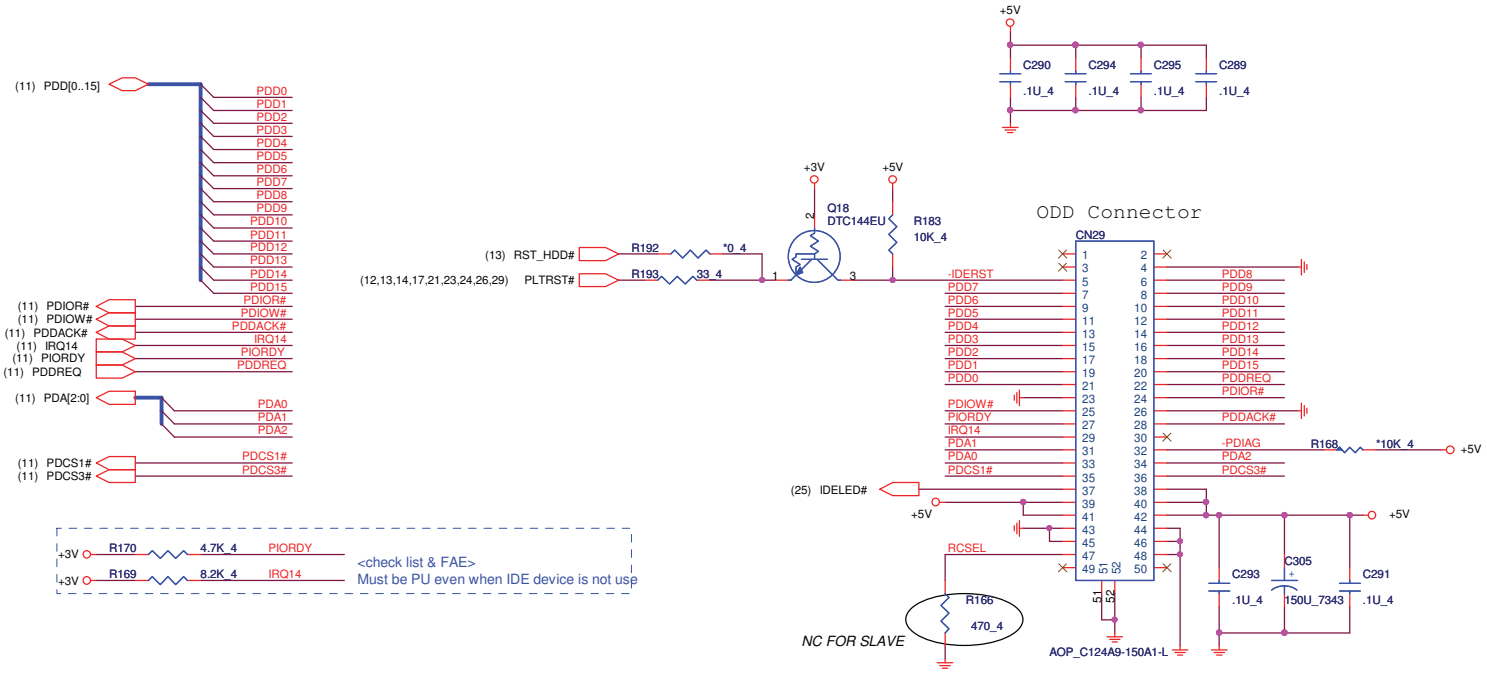
SATA HDD





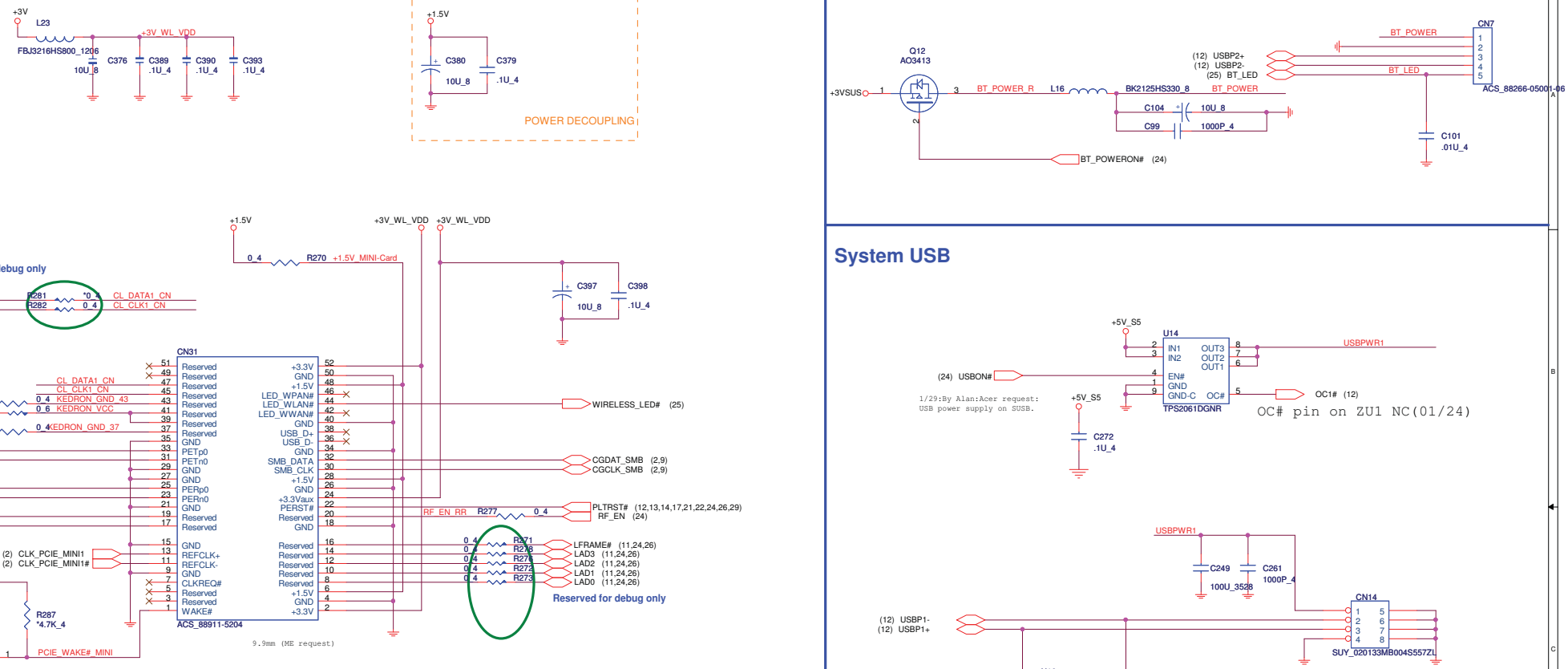


PATA ODD



PROJECT : ZU2		
Quanta Computer Inc.		
Size	Document Number: SATA-HDD & PATA-ODD	Rev: 1A
Date: Thursday, March 22, 2007	Sheet 22 of 39	

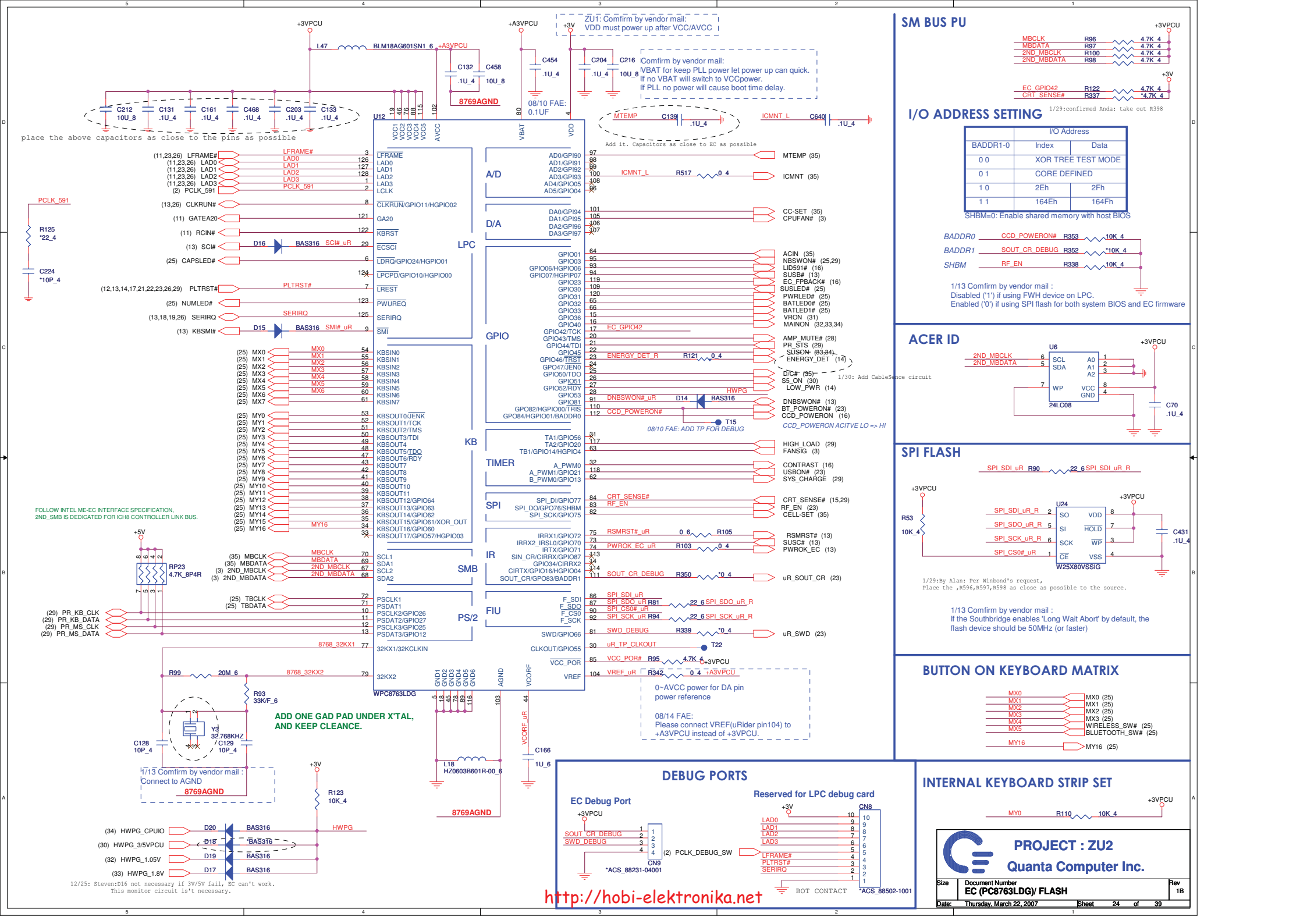
MINI-Card



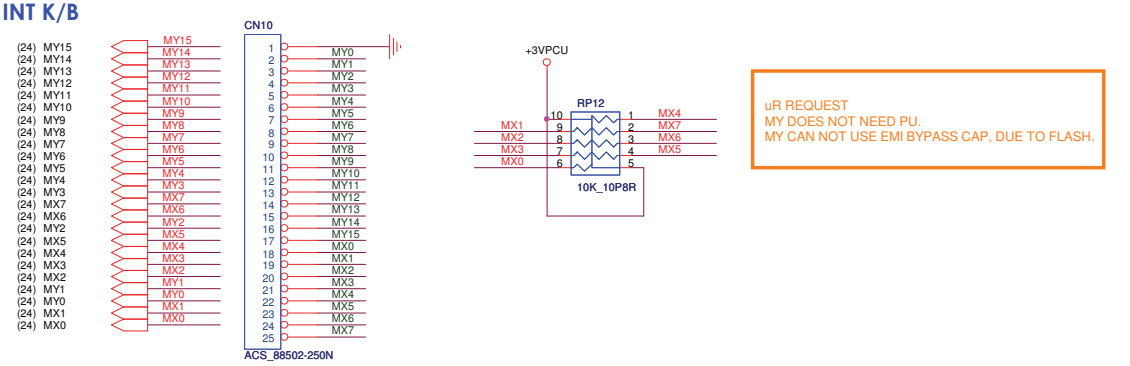
BLUETOOTH MODULE CONNECTOR

System USB

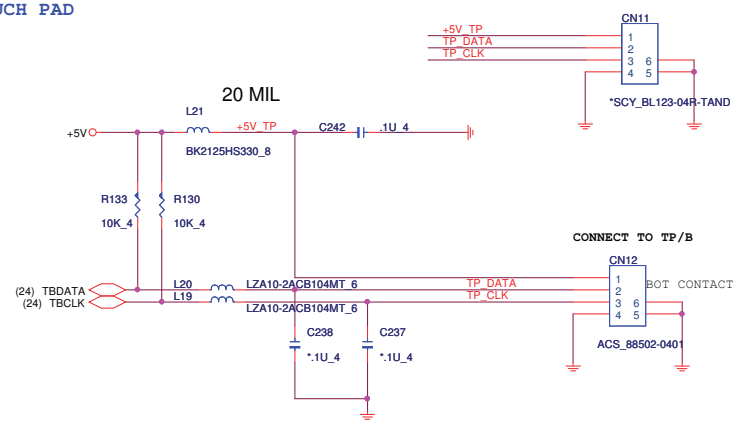
PROJECT : ZU2		
Quanta Computer Inc.		
Size	Document Number: Mini card/USB/Bluetooth	Rev: 1B
Date: Wednesday, March 28, 2007	Sheet 23 of 39	


ZU1: Comfirm by vendor mail:
VDD must power up after VCC/AVCC
Comfirm by vendor mail:
VBAT for keep PLL power let power up can quick.
If no VBAT will switch to VCCpower.
If PLL no power will cause boot time delay.
08/10 FAE:
0.1UF
place the above capacitors as close to the pins as possible
Add it. Capacitors as close to EC as possible
U12
WPC8763LDG
LPC
A/D
D/A
GPIO
KB
TIMER
SPI
SMB
IR
PS/2
FIU
FOLLOW INTEL ME-EC INTERFACE SPECIFICATION,
2ND_SMB IS DEDICATED FOR ICH8 CONTROLLER LINK BUS.
ADD ONE GAD PAD UNDER X'TAL,
AND KEEP CLEANCE.
1/13 Comfirm by vendor mail :
Connect to AGND
8769AGND
0~AVCC power for DA pin
power reference
08/14 FAE:
Please connect VREF(uRider pin104) to
+A3VPCU instead of +3VPCU.
08/10 FAE: ADD TP FOR DEBUG
CCD_POWERON ACITVE LO => HI
1/30: Add CableSence circuit
12/25: Steven:D16 not necessary if 3V/5V fail, EC can't work.
This monitor circuit isn't necessary.
SM BUS PU
I/O ADDRESS SETTING
SHBM=0: Enable shared memory with host BIOS
1/13 Comfirm by vendor mail :
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware
ACER ID
SPI FLASH
1/29:By Alan: Per Winbond's request,
Place the ,R596,R597,R598 as close as possible to the source.
1/13 Comfirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by default, the
flash device should be 50MHz (or faster)
BUTTON ON KEYBOARD MATRIX
DEBUG PORTS
EC Debug Port
Reserved for LPC debug card
INTERNAL KEYBOARD STRIP SET
http://hobi-elektronika.net
PROJECT : ZU2
Quanta Computer Inc.
EC (PC8763LDG)/ FLASH
Thursday, March 22, 2007
Sheet 24 of 39

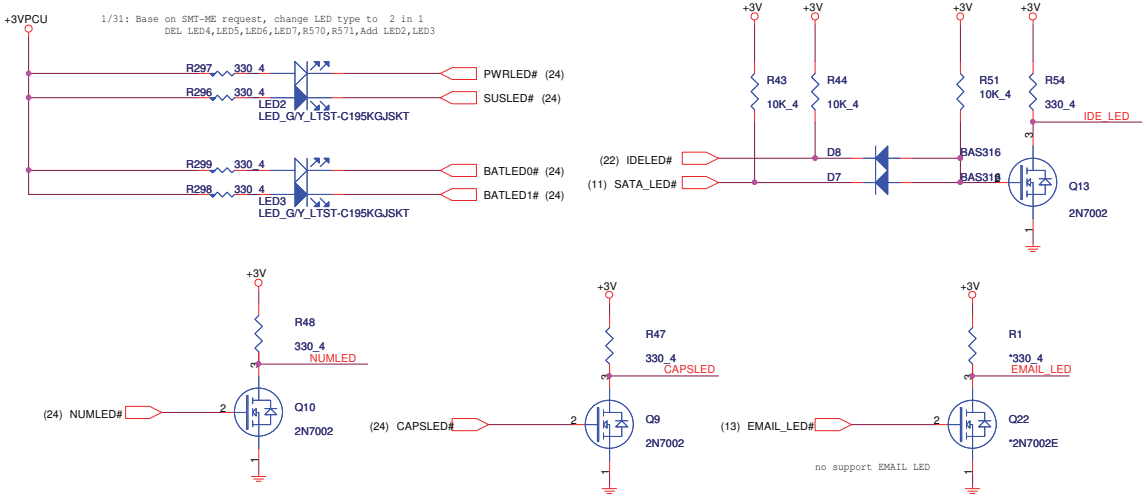
INT K/B



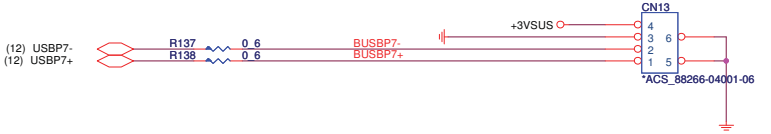
TOUCH PAD



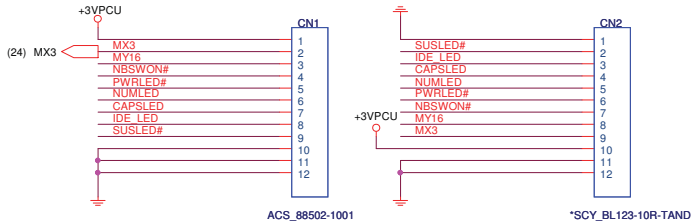
LED



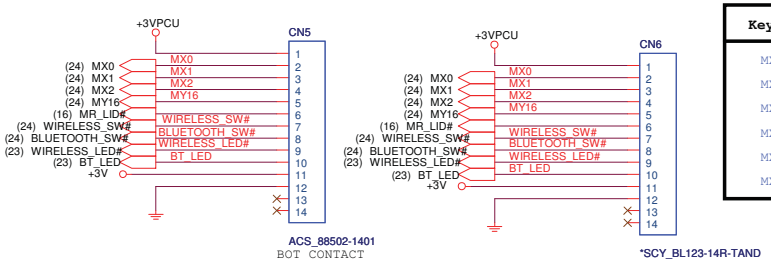
Finger Printer



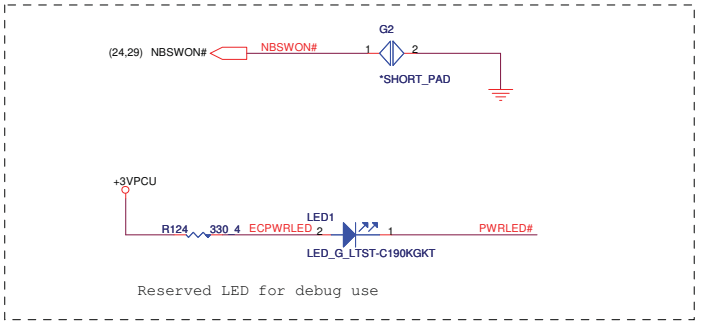
LED Board



Function Board



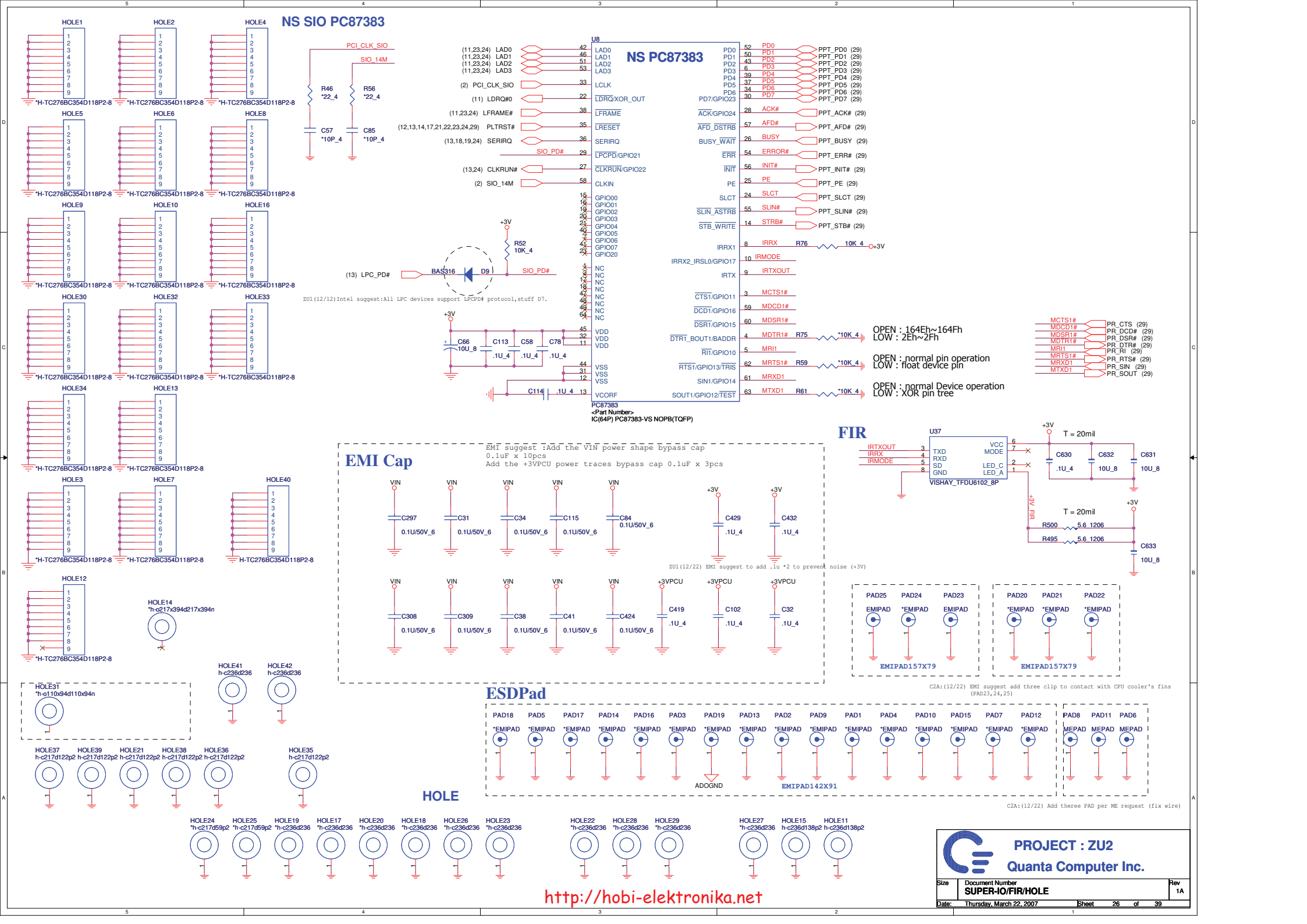
Keyboard Matrix	Button
MX0/MY16	acer EAP Buttton
MX1/MY16	acer EMAIL Buttton
MX2/MY16	acer WWW Buttton
MX3/MY16	acer EPM Buttton
MX4/MY16	WIRELESS Button
MX5/MY16	BLUETOOTH Button



PROJECT : ZU2
Quanta Computer Inc.

Size	Document Number	Rev
	SWITCH,LED,KB,Finger,TP	1B

Date: Tuesday, March 27, 2007 Sheet 25 of 39


NS SIO PC87383
NS PC87383
U8
PC87383
<Part Number>
IC(64P) PC87383-VS NOPB(TQFP)
ZU1(12/12)Intel suggest:All LPC devices support LPCPD# protocol,stuff D7.
OPEN : 164Eh~164Fh
LOW : 2Eh~2Fh
OPEN : normal pin operation
LOW : float device pin
OPEN : normal Device operation
LOW : XOR pin tree
FIR
U37
VISHAY_TFDU6102_8P
T = 20mil
EMI Cap
EMI suggest :Add the VIN power shape bypass cap
0.1uF x 10pcs
Add the +3VPCU power traces bypass cap 0.1uF x 3pcs
ZU1(12/22) EMI suggest to add .1u *2 to prevent noise (+3V)
EMIPAD157X79
C2A:(12/22) EMI suggest add three clip to contact with CPU cooler's fins (PAD23,24,25)
ESDPad
EMIPAD142X91
C2A:(12/22) Add theree PAD per ME request (fix wire)
HOLE
PROJECT : ZU2
Quanta Computer Inc.
Document Number
SUPER-IO/FIR/HOLE
Rev 1A
Date: Thursday, March 22, 2007
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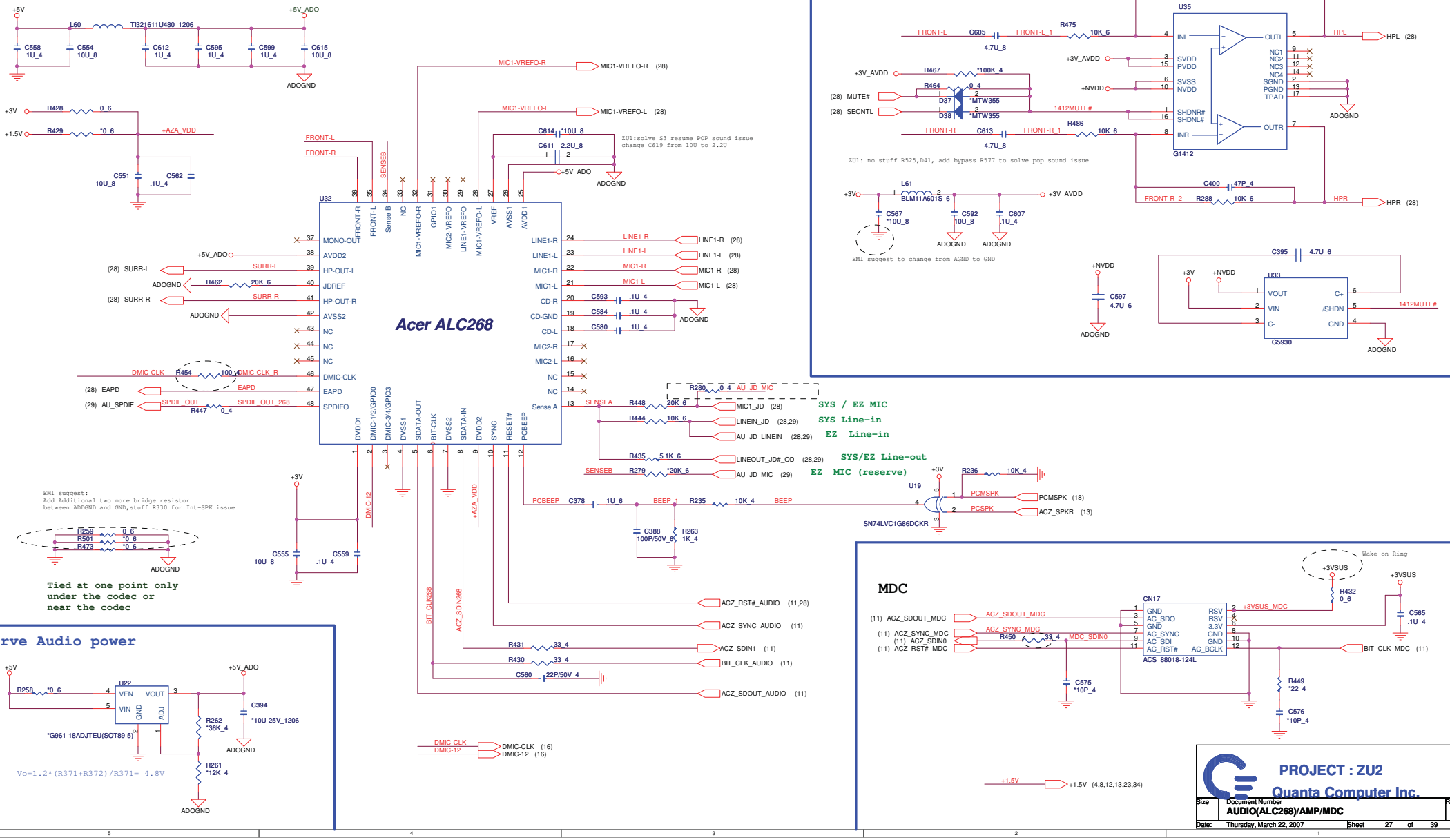
CODEC (ALC268)



LINE OUT Amplifier

Reserve Audio power

MDC

+1.5V (4,8,12,13,23,34)

PROJECT : ZU2
Quanta Computer Inc.

Size	Document Number	Rev
	AUDIO(ALC268)/AMP/MDC	1A
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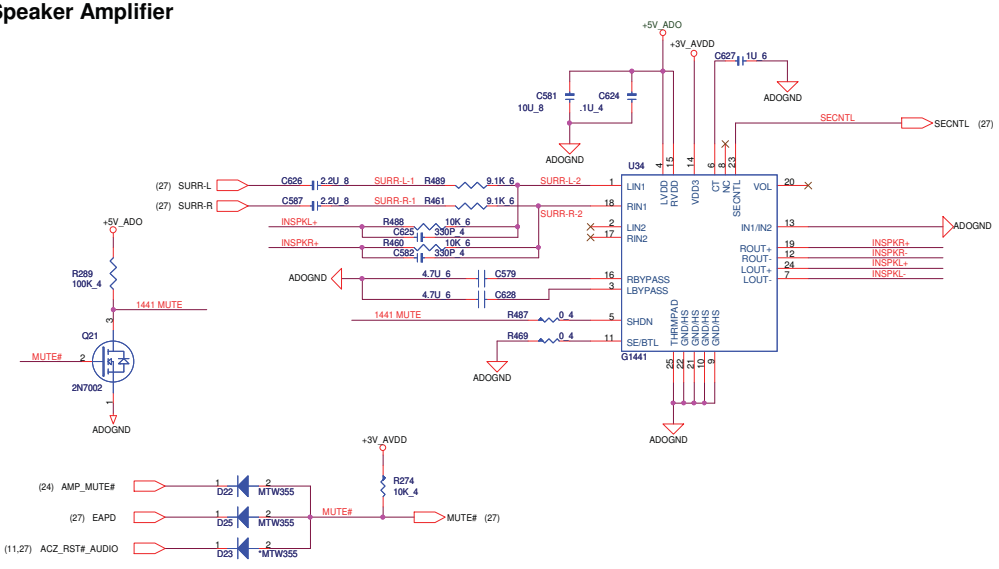
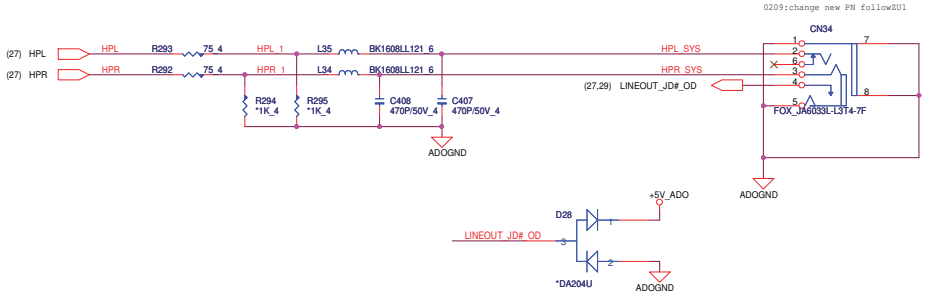
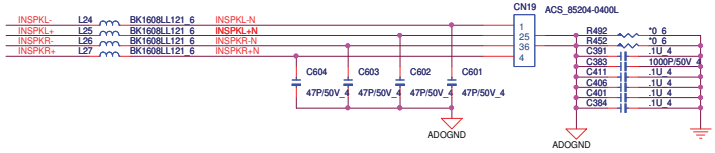
Speaker Amplifier



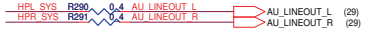
SYSTEM LINE OUT



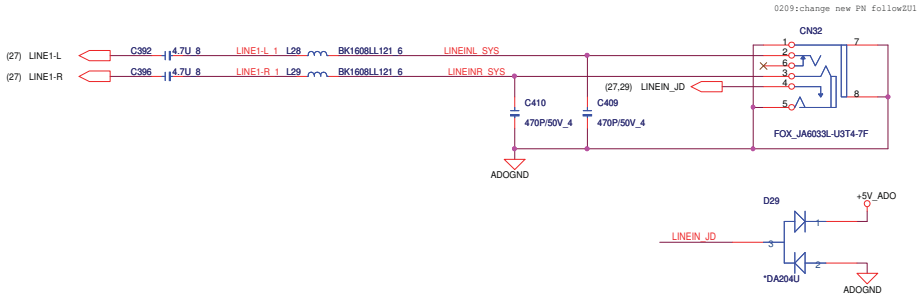
SPEAKER



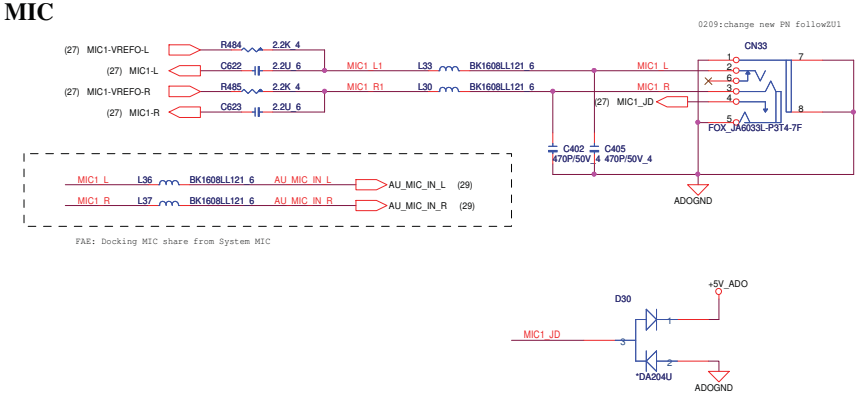
Docking LINE OUT/SPDIF



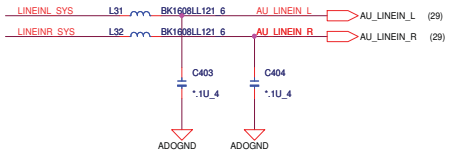
SYSTEM LINE IN



SYSTEM MIC



Docking LINE IN



PROJECT : ZU2
Quanta Computer Inc.

Size	Document Number	Rev
	Speaker AMP / Audio JACK	1A
Date: Thursday, March 22, 2007	Sheet 28 of 39	

3/16 Modify D5 Footprint from SBM1040-3P to SBM1040-3P-ZU1

1/31:Acer DVR1012_Design Requirement Checklist:
The system side should have a diode
to block the AC adaptor power coming from ezDock.

D5 PDS1040S

D10 SW1010C

CN25 FOX_QL0177L-D26C02-8F

EMI suggest add 10u*1pc, 0.1u*5pcs

POWER DECOUPLING

ZU1: Add PL 100K for DVI_DET

A1A:(11/1) Change LAN pin define

(1)Remove Level-shift circuit (already in docking side)
(2)change Power from +3V to +2.5V
(3)stuff 2.2k (R374,R375)

add level shift circuit, already PU 5VA_PR in docking side.
add R566 0ohm for debug use

Refer to Acer DVR1019

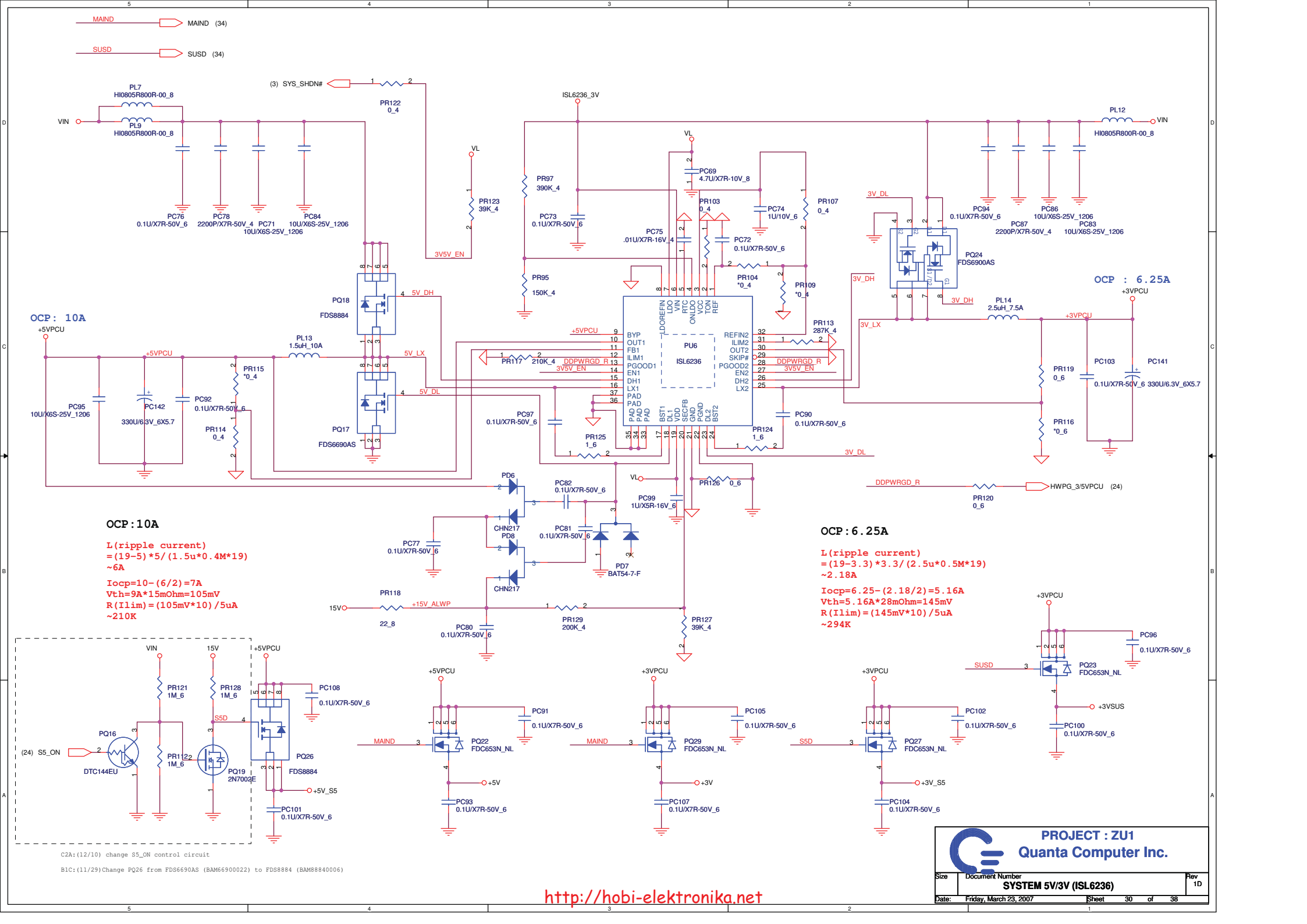
ZU1:Add R and C between
AUDIO_AGND and GND

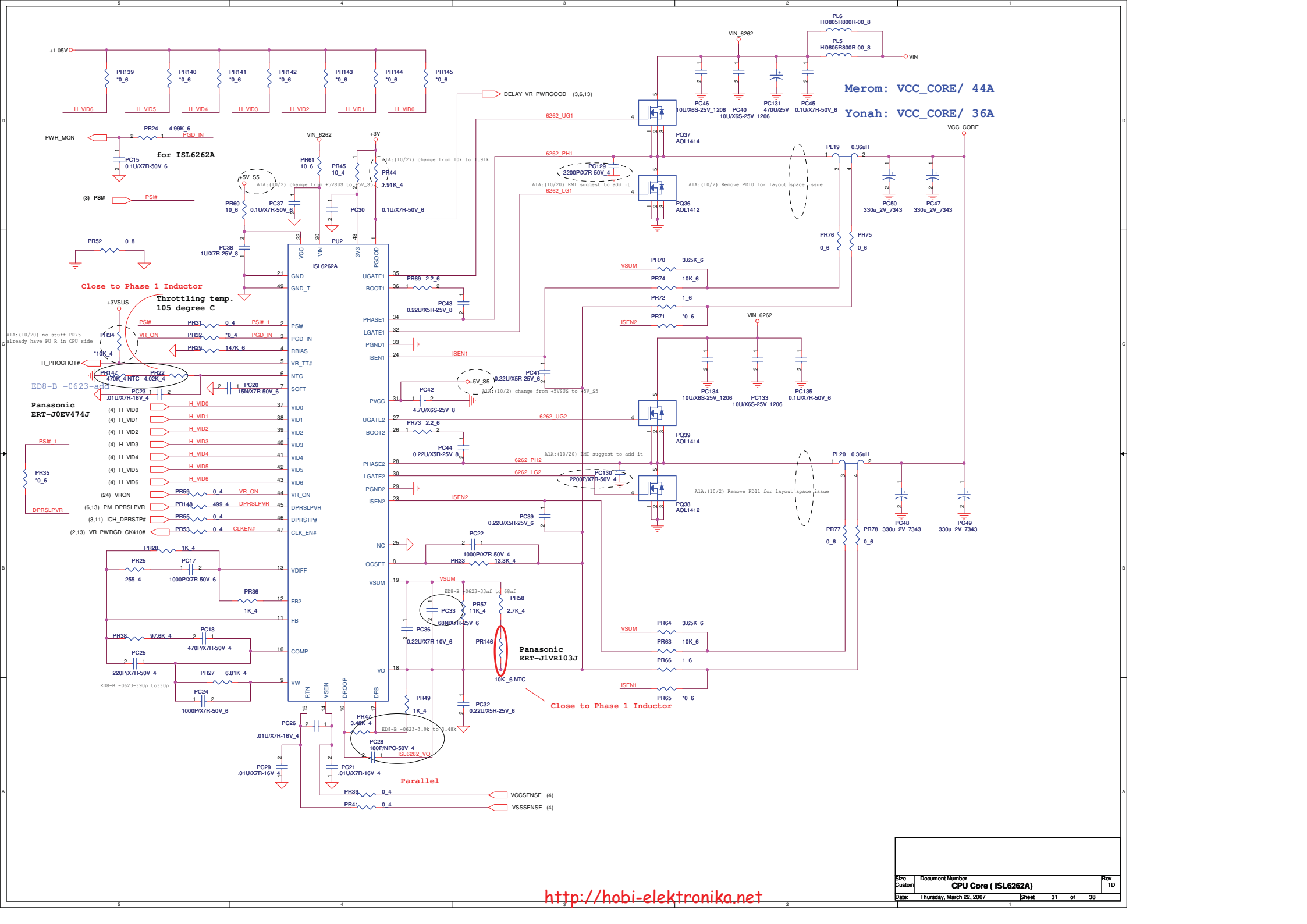
EMI suggest to add .1u to prevent noise

refer to Acer Design Guide:
this signal is asserted to power on the system.
A buffer used for PWRBTN# on the system side
may be necessary to prevent the signal interfered
by the contact noise.

PROJECT : ZU2
Quanta Computer Inc.

Size	Document Number	Rev
	Docking(ezDockII/II+)	1B
Date: Friday, March 23, 2007	Sheet 29 of 39	

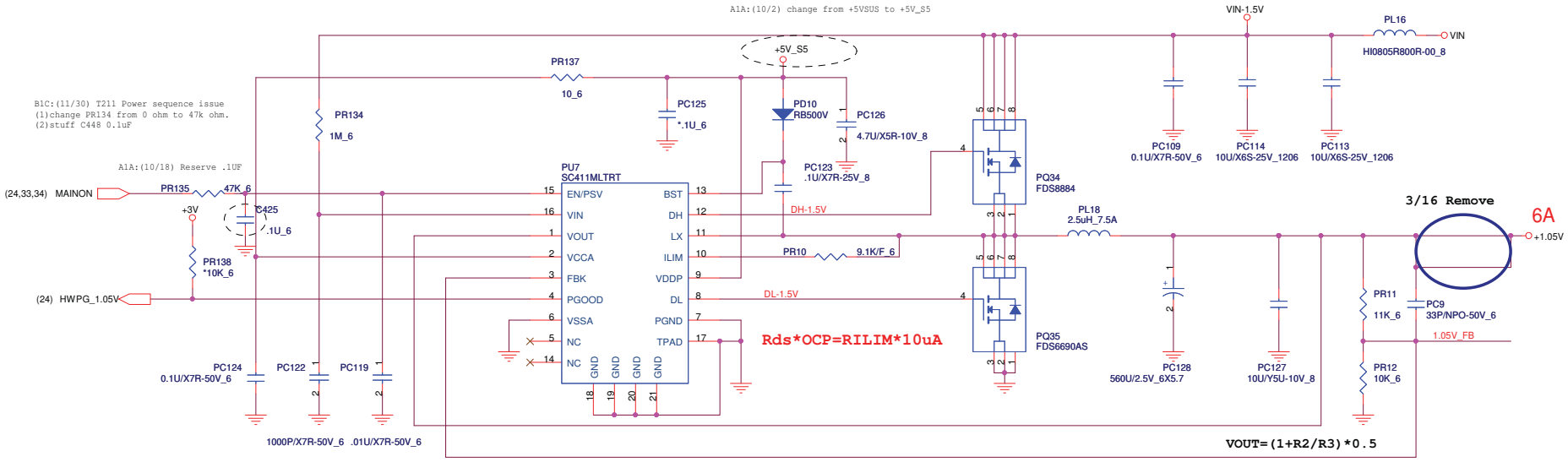



Merom: VCC_CORE/ 44A
Yonah: VCC_CORE/ 36A
for ISL6262A
Close to Phase 1 Inductor
Throttling temp.
105 degree C
Panasonic
ERT-J0EV474J
Panasonic
ERT-J1VR103J
Close to Phase 1 Inductor
Parallel
ISL6262A
VCC_CORE
http://hobi-elektronika.net
CPU Core (ISL6262A)
Thursday, March 22, 2007

A1A:(10/2) change from +5VSUS to +5V_S5

B1C:(11/30) T211 Power sequence issue
(1)change PR134 from 0 ohm to 47k ohm.
(2)stuff C448 0.1uF

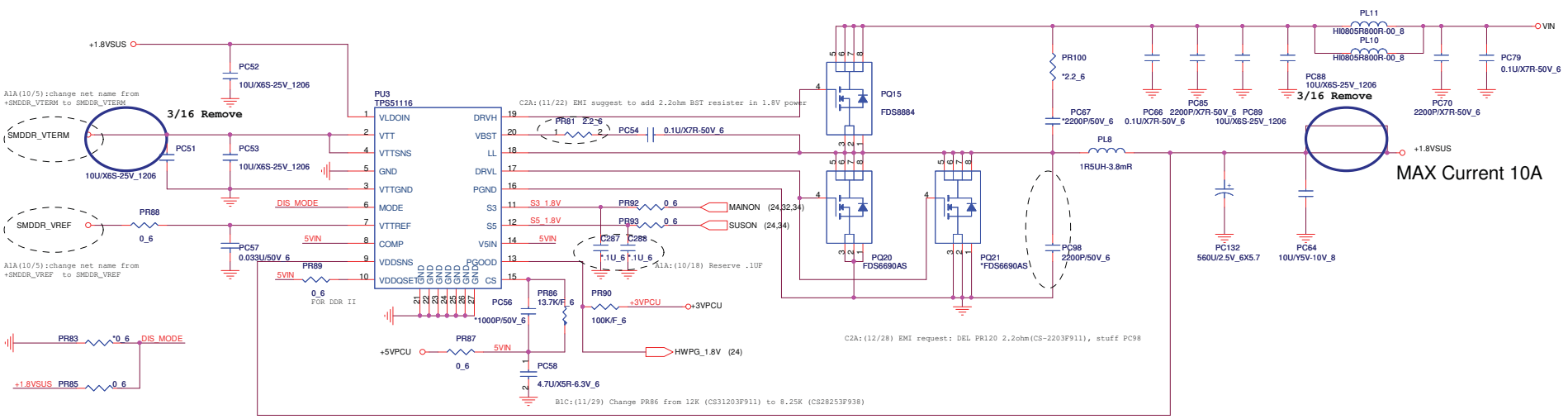
A1A:(10/18) Reserve .1UF



B1C:(11/29) Change PR8 from 20K(CS32003F933) to 6.65K ohm (CS26653F911)

PROJECT : ZU1
Quanta Computer Inc.

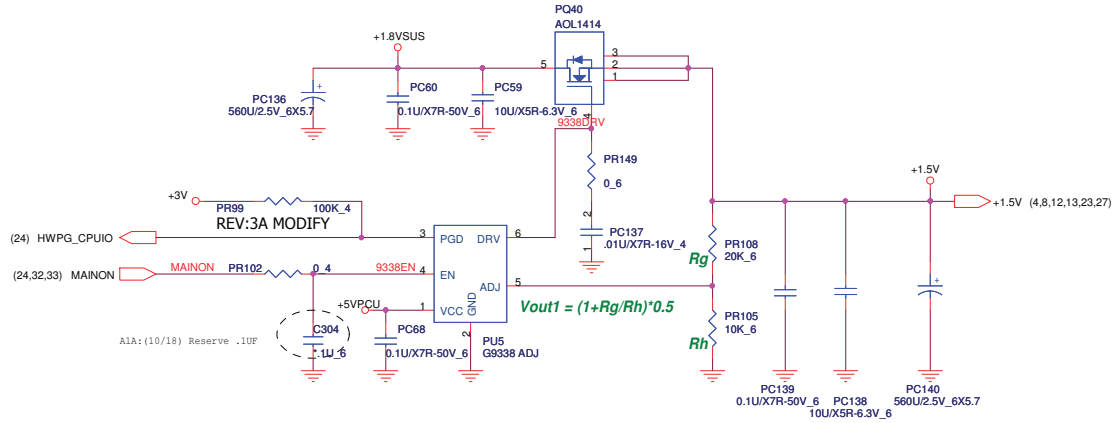
Size	Document Number	Rev
	VTT 1.05V (SC411)	1D
Date: Thursday, March 22, 2007	Sheet 32 of 38	

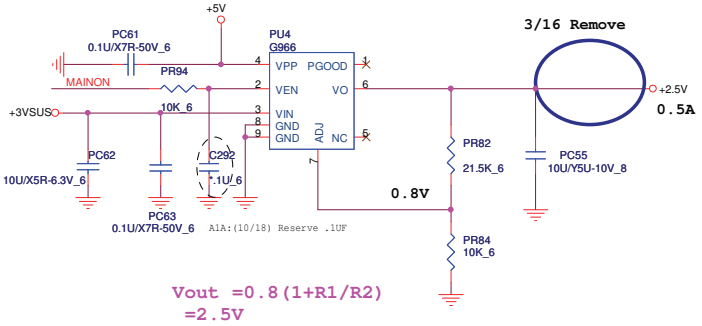


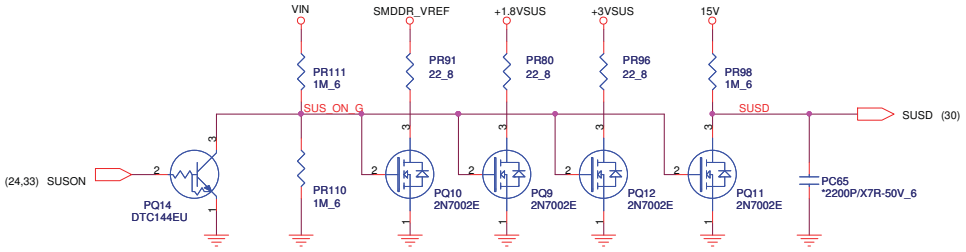
A1A(10/5):Remove +1.8V circuit

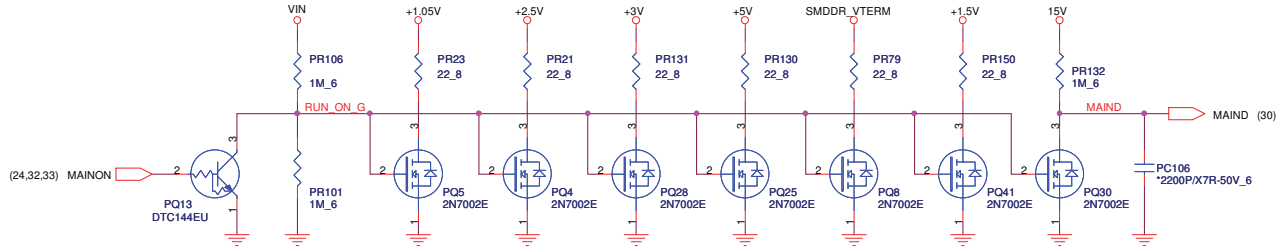
PROJECT : ZU1
Quanta Computer Inc.

Size	Document Number	Rev
	DDR 1.8V(TPS51116)	1D
Date: Thursday, March 22, 2007	Sheet 33 of 38	









PROJECT : ZU1
Quanta Computer Inc.

Size	Document Number	Rev
	Discharge (1.5V/2.5V)	1D
Date: Thursday, March 22, 2007	Sheet 34 of 38